

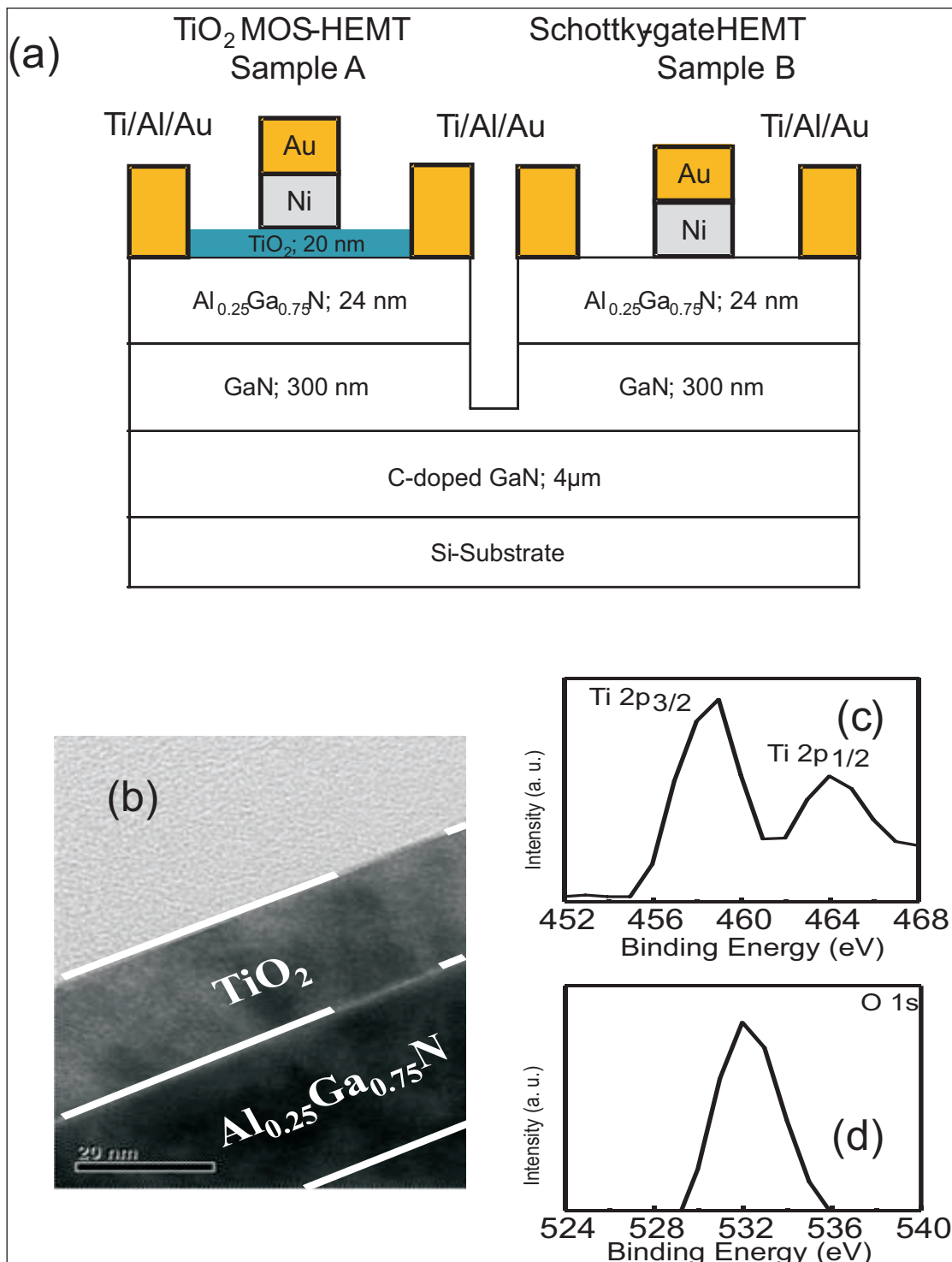
First application of low-cost deposition of titanium dioxide for GaN MOS-HEMT

Ultrasonic spray pyrolysis deposition has been used to create devices with promising performance characteristics.

Researchers in Taiwan have used ultrasonic spray pyrolysis deposition (USPD) "for the first time" to apply titanium dioxide (TiO_2) high-k dielectric layers to aluminium gallium nitride ($\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$) metal-oxide-semiconductor high-electron-mobility transistors (MOS-HEMTs) [Bo-Yi Chou et al, IEEE Electron Device Letters, published online 17 September 2014].

The team — from National Cheng Kung University, Feng Chia University, and Industrial Technology Research Institute — sees USPD as an economical deposition method. In particular, the non-vacuum process environment and high deposition rate make USPD suitable for low-cost large-area deposition and other mass-production scenarios.

Figure 1. (a) Schematic diagram of AlGaN/GaN MOS-HEMT, (b) transmission electron microscope photo of MOS-gate structure, and (c) electron spectroscopy for chemical analysis (ESCA) intensities.



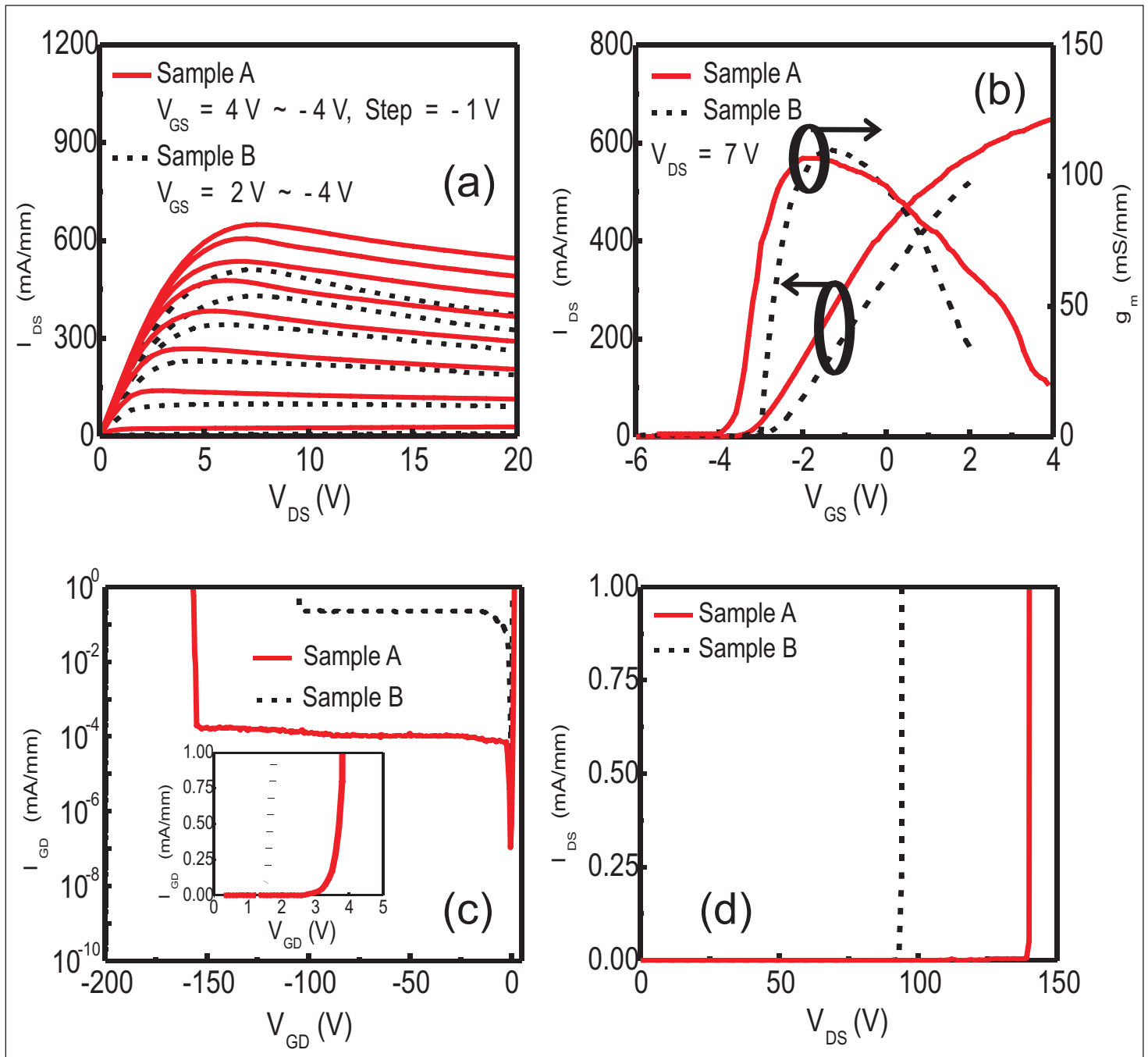


Figure 2. (a) Common-source I_{DS} - V_{DS} curves, (b) transfer g_m/I_{DS} , (c) two-terminal off-state I_{GD} - V_{GD} , and (d) BV_{DS} characteristics at 300K.

USPD has previously been used to create aluminium oxide dielectric layers for GaN MOS-HEMTs. TiO_2 has a higher dielectric constant of 86–173, compared with ~ 10 for aluminium oxide.

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low-pressure metal-organic chemical vapor deposition (LP-MOCVD) on silicon (see Figure 1). The MOS-HEMT fabrication involved mesa etching for electrical isolation, titanium/aluminium/gold deposition and annealing for ohmic source-drain contacts, 20nm TiO_2 USPD for gate insulation, exposure of the source-drain electrodes, and nickel/gold deposition for the gate electrode. A reference Schottky-gate device was produced without TiO_2 dielectric.

The gate length and width were $1\mu m$ and $100\mu m$, respectively. The gate-source and gate-drain spacings were both $2\mu m$.

Hall measurements before and after TiO_2 USPD gave carrier densities of $2.08 \times 10^{13}/cm^2$ and $2.41 \times 10^{13}/cm^2$,

Table 1. Comparison of MOS-HEMT and Schottky HEMT.

	MOS-HEMT	Schottky HEMT
Maximum drain current	650mA/mm	511mA/mm
Maximum drain current at 0V gate	384mA/mm	342mA/mm
Peak transconductance	107mS/mm	110mS/mm
Gate voltage swing	2.7V	1.7V
Two-terminal gate-drain breakdown voltage (BV_{GD})	-155V	-105V
On voltage	3.8V	1.8V
On-state breakdown (BV_{DS})	139V	94V
On/off current ratio	4.5×10^5	3.5×10^2

respectively. The mobility slightly decreased, respectively, from $883\text{cm}^2/\text{V}\cdot\text{s}$ to $872\text{cm}^2/\text{V}\cdot\text{s}$. The product of carrier density and mobility was increased from $1.84 \times 10^{16}/\text{V}\cdot\text{s}$ to $2.1 \times 10^{16}/\text{V}\cdot\text{s}$, leading to expectations of increased on-current with TiO_2 gate insulation/passivation.

Capacitance versus voltage (CV) measurement gave an oxide capacitance of 190pF and a dielectric constant (k) of 53.6, lower than the range quoted above. The composition of the USPD ' TiO_2 ' was estimated as a Ti/O ratio of 0.47, which is slightly off the 0.5 for exact TiO_2 . The equivalent oxide thickness (EOT) of the 20nm TiO_2 layer was estimated at 1.45nm.

The threshold voltage of the MOS-HEMT was negative (normally-on, depletion-mode) at -3.9V. At zero gate potential the maximum drain current (I_{DSS0}) was 384mA/mm for the MOS-HEMT and 342mA/mm for the Schottky HEMT. The researchers also compared their devices with those produced using different TiO_2 deposition techniques. USPD gave "the best improvement [over Schottky-based devices] of I_{DS} at $V_{GS} = 0\text{V}$ (ΔI_{DSS0}) of 12.3%, the highest G_{VS} linearity of 2.7V, enhanced $g_{m,max}$, and superior low I_{GD} leakage".

The electrical performance between the devices was compared, generally showing improved performance of the MOS-HEMT over the Schottky HEMT (see Figure 2 and Table 1). The maximum drain current (I_{DS}) of the MOS-HEMT was 650mA/mm. The peak transconductance ($g_{m,max}$) was 107mS/mm. The reference Schottky HEMT had corresponding performance values of 511mA/mm and 110mS/mm. The increased gate-channel separation in the MOS-HEMT device only slightly decreased the peak transconductance due to use of TiO_2 as a high-k dielectric with its 1.45nm EOT.

The gate voltage swing (G_{VS}) linearity for transconductance within 90% of the peak value was 2.7V for the MOS-HEMT, compared with 1.7V for the Schottky HEMT.

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The researchers also compared their devices with those produced using different TiO_2 deposition techniques (Table 2), commenting that USPD gave "the best improvement [over Schottky-based devices] of I_{DS} at $V_{GS} = 0\text{V}$ (ΔI_{DSS0}) of 12.3%, the highest G_{VS} linearity of 2.7V, enhanced $g_{m,max}$, and superior low I_{GD} leakage". ■

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Table 2. Comparisons with other TiO_2 -dielectric MOS-HEMTs.

Oxidation technique	USPD	Liquid phase deposition	Molecular beam epitaxy	Evaporation
Gate length	1 μm	1 μm	0.7 μm	0.5 μm
Dielectric constant, k	53.6	24.4	70	80
ΔI_{DSS0}	12.3%	-7.8%	-6%	-67%
$\Delta g_{m,max}$	-2.7%	-1%	-20.9%	-50%
$g_{m,max}$	(110mA/mm)	(99mA/mm)	(140mA/mm)	(60mA/mm)
G_{VS} (V)	2.7V	2.2V	2V	2.4V
I_{GD} @ $V_{GD} = -50\text{V}$	1×10^{-4} mA/mm	1×10^{-4} mA/mm	8×10^{-3} mA/mm	