Expanding interest in cubic silicon carbide on silicon substrates

SiC on Si substrates could reduce costs for power electronics and III-nitride LEDs, reports Mike Cooke.

Silicon carbide (SiC) is widely developed and promoted as a semiconductor material for high-power and high-temperature electronics. Additional advantages include high thermal conductivity and fast switching speeds. Further, a close lattice match to gallium nitride (GaN) and high thermal conductivity make SiC an attractive substrate for high-power blue and ultraviolet LEDs. The well known drawback of SiC is the high cost of high-quality substrates.

Table 1. Some material characteristics of various polytypes of SiC and of Si from www.ioffe.ru/SVA/NSM/Semicond/SiC/ebasic.html and www.ioffe.ru/SVA/NSM/Semicond/Si/electric.html

	3C-SiC	4H-SiC	6H-SiC	Si
Breakdown field	10^6V/cm	(3–5)x10^6V/cm	(3–5)x10^6V/cm	3x10^5V/cm
Electron mobility	≤800cm^2/V-s	≤900cm^2/V-s	≤400cm^2/V-s	≤1400cm^2/V-s
Hole mobility	≤320cm^2/V-s	≤120cm^2/V-s	≤90cm^2/V-s	≤450cm^2/V-s

An alternative route to SiC electronics – epitaxial growth on silicon — has been around since the 1990s. This potentially allows large-scale production on wafers up to 300mm diameter, compared with 150mm for bulk SiC substrates offered by commercial suppliers such as Cree of Durham, NC, USA. MTI Corp of Richmond, CA, USA is one commercial supplier of 3C-SiC on Si wafers with a diameter of up to 8-inch (200mm). In 2013, Queensland Micro and Nanotechnology Facility (QMF) of Griffith University in Australia claimed the first 3C-SiC on 300mm Si wafers.

Developers of 3C-SiC on Si see opportunities beyond electronic devices such as micro-electro-mechanical systems (MEMS) and as substrate/buffer layer for the growth of III-nitride materials and graphene. In fact, Linköping University in Sweden found in 2013 that large-area 50\micronx50\micron graphene sublimated on 3C-SiC demonstrated superior uniformity over graphene on 4H- and 6H-SiC. (Linköping has also developed a 3C-SiC growth technology that uses 6H-SiC substrates.)

However, 3C-SiC on Si has a different crystal structure (polytype) from bulk SiC substrates: respectively, cubic — the '3C' — rather than hexagonal 4H/6H (Table 1). Supporters argue that 3C-SiC has many advantages for MOS device applications due to a smaller energy bandgap, which is associated with higher mobility in general. The electron Hall mobility for 3C-SiC is also not direction dependent (i.e. 'isotropic'), unlike the mobility in 4H/6H SiC. The narrower bandgap also means a reduced ability to handle high electric fields – a feature not so desirable for power devices.

QMF has been working on low-temperature 3C-SiC/Si for more than 10 years. The facility worked with equipment-making company SPTS Technologies Ltd of Newport, Wales, UK on the reactor for the deposition on 300mm wafers. QMF and SPTS hope that their joint work will lead to a cost-effective buffer for GaN devices on silicon substrates. Cost analyses suggest that the process should add no more than $35 to the cost of 300mm substrates. QMF claims 1% uniformity in SiC layer thickness across 300mm wafers.

Researchers at QMF and Queensland University of Technology have also explored different ways to reduce surface roughness, such as chemical mechanical polishing (CMP) and plasma etching. In 2014, the team achieved nanometer-scale roughness with CMP removal of 200nm of the 3C-SiC layer. Hydrogen chloride plasma gave a 30% improvement in roughness, sacrificing only 50nm of the 3C-SiC. QMF has also researched potential MEMS and III-nitride applications.

Processing of 3C-SiC needs lower temperatures than for 4H/6H materials. This should allow the use of more standard silicon-like device fabrication, such as room-temperature ion implantation. At the same time, 3C-SiC has an improved critical electric field over silicon,

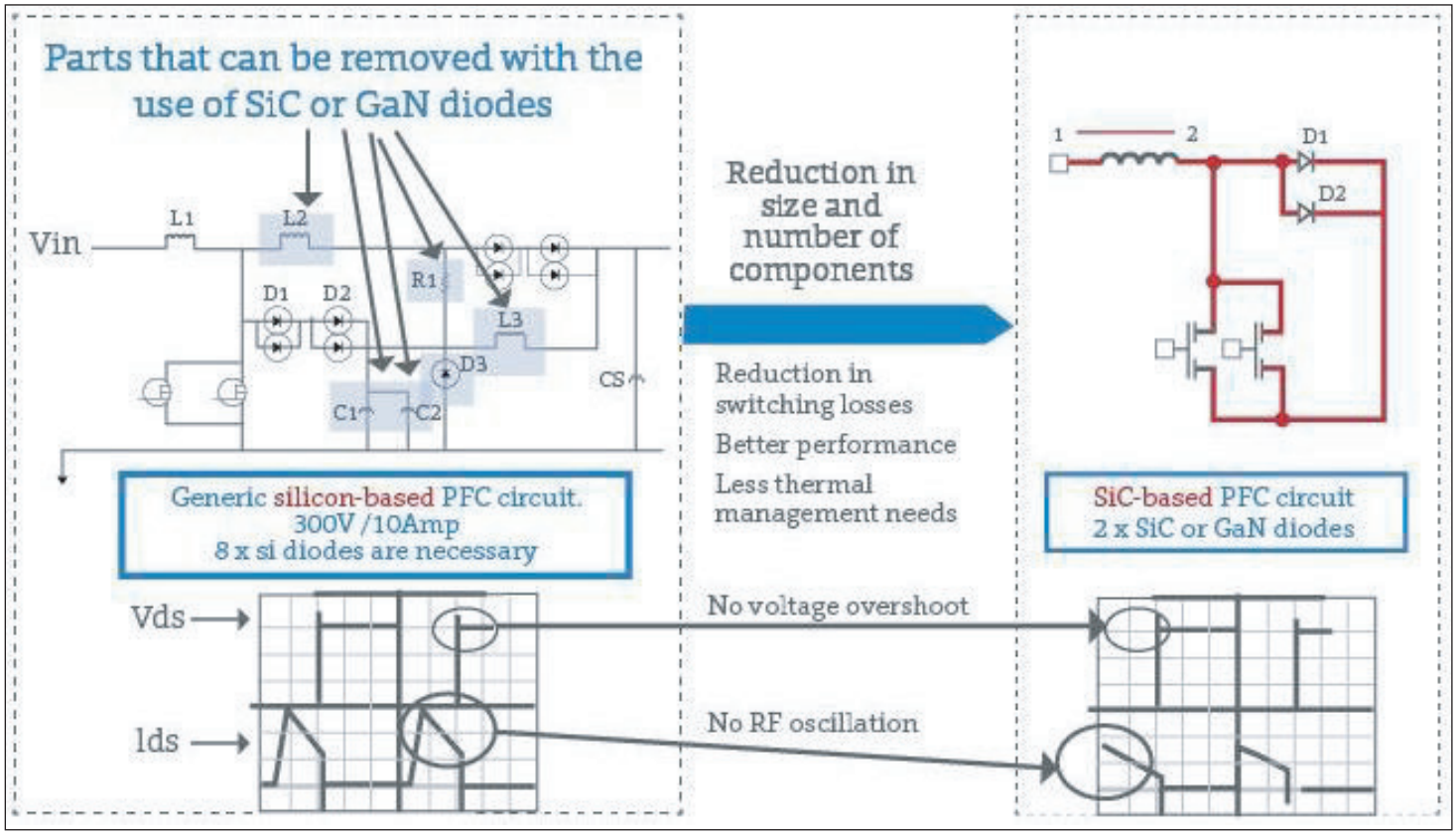

Figure 1. Anvil case study — use of 3C-SiC in power factor correctors.

so that expensive and challenging 'super-junction' processes are not needed.

There are challenges, of course. Standard growth of 3C-SiC on Si through low-pressure chemical vapor deposition (LPCVD) needs substrate temperatures around 1350ºC or higher — close to silicon's melting point. High temperature also redistributes dopants and accumulates thermal mismatch stress.

Anvil Semiconductors Ltd of Coventry, UK claims 'unique technology' for growing 3C-SiC on silicon that reduces SiC wafer costs by a factor of 20. The epitaxial process includes patented stress control techniques to overcome lattice and thermal expansion mismatches between 3C-SiC and silicon.

The Anvil technique uses a polycrystalline SiC grid to divide the wafer into squares, reducing the effect of lattice mismatch and thermal expansion. The square crystal SiC regions are still large enough for complex devices. The company has demonstrated thick epitaxial layers up to around 10\micron on 100mm-diameter wafers. When stress accumulates in epitaxial processes the wafers tend to bend/bow — Anvil reports that its processed wafers are 'without bow'. The company expects that its process can be readily migrated to 150mm Si wafers and beyond.

The company believes that its process will lead to production of silicon carbide (SiC) power switches at a similar cost to devices on conventional silicon. Vertical Schottky barrier diodes (SBDs) and metal-oxide-semiconductor field-effect transistors (MOSFETs) with 650V and 1200V ratings can be realized with the material, according to Anvil. Such devices could lead to a reduction in the number and size of components needed in power systems (Figure 1).

Anvil was established in August 2010 based on technology and personnel from Warwick University. In 2013, Anvil secured £1m in funding from a number of investors to accelerate development and commercialization of the technology. The investors were led by the part-EU-funded Low Carbon Innovation Fund (LCIF); other backers were Ntensive, Cambridge Capital Group, Midven and Minerva Business Angels, along with several individuals.

This funding was followed up in 2014 with a grant from the UK Technology Strategy Board (now Innovate UK) to evaluate the feasibility of using Anvil's 3C-SiC/Si technology to enable the production of low-cost, high-brightness LEDs on large-diameter silicon substrates.

Although attempts have been made to grow GaN LEDs directly on silicon, the poor matching of the lattices and thermal expansion coefficients make it difficult to achieve the high-quality material needed for efficient LEDs. Silicon carbide has a better lattice and thermal expansion match with GaN.

Anvil hopes its SiC/Si process will lead to better-quality GaN layers on silicon at low cost. Further, the research team wanted to explore the possibility of producing non-polar cubic (zinc blende) GaN. Normal hexagonal wurtzite GaN has strong spontaneous and strain-dependent (piezoelectric) polarization due to the

partially ionic character of the chemical bond. The polarization can lead to strong electric fields in the III-nitride heterostructures used to make LEDs. These electric fields reduce the recombination of electrons and holes into photons, adversely affecting LED efficiency.

In fact, successful production of cubic GaN on 3C-SiC was announced in December 2014. Anvil and University of Cambridge's Center for GaN report that single-phase GaN was produced on 3C-SiC/Si using metal-organic chemical vapor deposition (MOCVD). "The layers, characterized by XRD, TEM, photoluminescence and AFM, show promise for LED applications," according to Anvil.

Like 3C-SiC, cubic GaN has a narrower bandgap than its hexagonal counterpart (about 0.2eV less, according to www.ioffe.ru/SVA/NSM/Semicond/GaN/bandstr.html). Also, holes have improved transport properties in cubic GaN. Poor hole transport has been one of the roadblocks to more efficient GaN LEDs.

University of Cambridge professor Sir Colin Humphreys commented: "This is a very promising development and fits well with our current research activities to develop state-of-the-art LEDs. It has the potential to overcome many of the challenges currently seen for green devices and could contribute significantly to the ongoing solid-state lighting revolution."

Anvil has made a production source agreement with commercial SiC wafer and epitaxy supplier Norstel AB. It announced in September 2014 that its 3C-SiC/Si process had been successfully transferred onto production reactors at Norstel's facilities in Norrkoping, Sweden. The move enables the technology to progress to 150mm (6-inch) wafers.

Anvil has also been contributing to a Raytheon-led project developing robust, high-temperature driver circuits for power transistors using low-cost 3C on Si. Part of the funding also comes from the UK Technology Strategy Board. The work has been ongoing from October 2012 to September 2015 at Raytheon's facility in Glenrothes, Scotland, UK. The research is particularly focused on driver circuits for energy-efficient power transistors operating at high temperature that could find application in oil and gas exploration, energy generation and electric vehicles.

Universität Paderborn in Germany has used 3C-SiC on Si substrates for plasma-assisted molecular beam epitaxy (PAMBE) of cubic GaN, AlN and AlGaN alloys [Donat J. As and Christian Mietze, Phys. Status Solidi A 210, p474, 2013]. The researchers developed quantum wells of cubic III-N material with photoluminescence peaks from inter-sub-band transitions in the optical communication 1.3–1.5μm wavelengths. Some of this work used free-standing 3C-SiC substrates (i.e. material with the Si growth substrate removed).

The researchers see the growth of non-polar cubic GaN/AlN multi quantum well (MQW) structures on (001)-oriented substrates that eliminate the detrimental strong spontaneous polarization fields as possibly allowing easier design of complex structures such as for quantum cascade lasers (QCLs).

Italy's Institute for Microelectronics and Microsystems (IMM-CNR) and Catania Epitaxial Technology Center, along with University of Florida in the USA, have tried to improve 3C-SiC quality by surface texturing the silicon growth wafer with inverted square-base pyramids [Francesco La Via, et al, Journal of Materials Research, vol28, p94, 2013].

The texturing resulted in stacking faults combining within the first micron of growth, reducing the stacking fault density to $9.31 \times 10^3/cm^3$ in 9μm-thick 3C-SiC layers. Lower residual stress in the 3C-SiC samples on textured substrate was attributed to faster stress relaxation during growth.

Gallium nitride transistors

Researchers in Germany have developed GaN high-electron-mobility transistors (HEMTs) on silicon carbide (SiC) layers on silicon wafers [Wael Jatal et al, IEEE Electron Device Letters, published online 11 December 2014]. The ohmic source-drain contacts were gold-free (Au-free) titanium nitride on titanium (TiN/Ti). The researchers came from Technische Universität Ilmenau and Institut für Mikroelektronik- und Mechatronik-Systeme gemeinnützige GmbH (IMMS GmbH).

GaN-based HEMTs are being developed for radio frequency (RF) power amplification, based on high operating frequencies combined with high output power. The best GaN transistors are generally produced on 4H-SiC wafers.

The substrate used by Jatal et al was low-resistivity (3mΩ-cm) (111) Si on which 3C-SiC had been deposited. RF applications usually prefer semi-insulating or fully insulating wafers to reduce factors such as substrate leakage and signal cross-talk.

The SiC growth began with 3nm carbonization with ethylene (C_2H_4) precursor. Further SiC was grown by adding silane (SiH_4) as a silicon chemical vapor deposition (CVD) precursor. MOCVD was then used to apply 100nm aluminium nitride (AlN) as an interlayer, and GaN buffer. The barrier structure consisted of $Al_{0.2}Ga_{0.8}$/AlN (design A) or $Al_{0.35}Ga_{0.65}N$ (design B). The AlGaN barrier thickness in both cases was 20nm. The AlN spacer between the AlGaN barrier and GaN buffer of design A was 2nm. The structures were capped with 2nm of GaN.

The epitaxial design A achieved a Hall mobility of $1760cm^2/V\text{-}s$, compared with $1200cm^2/V\text{-}s$ for design B. The sheet carrier densities were very similar, at $7.5 \times 10^{12}/cm^2$ for design A and $7.2 \times 10^{12}/cm^2$ for design B.

The nickel-gold HEMT gate had two fingers of total width 150μm. The gate was centered in the 2μm source-drain gap.

The ohmic contacts for the source-drain regions were applied using magnetron sputtering of titanium. The initial deposition was 20nm of titanium followed by 100nm of titanium nitride. The titanium nitride was formed through reactive magnetron sputtering in an argon/nitrogen atmosphere and annealing at 850ºC in nitrogen.

The specific contact resistance of the Ti/TiN structures was ~10^{-6}Ω-cm^2. The contact resistance was 0.13Ω-mm. The root-mean-square (rms) roughness was 1.8nm. The researchers claim that their Ti/TiN structure is among the best gold-free structures so far.

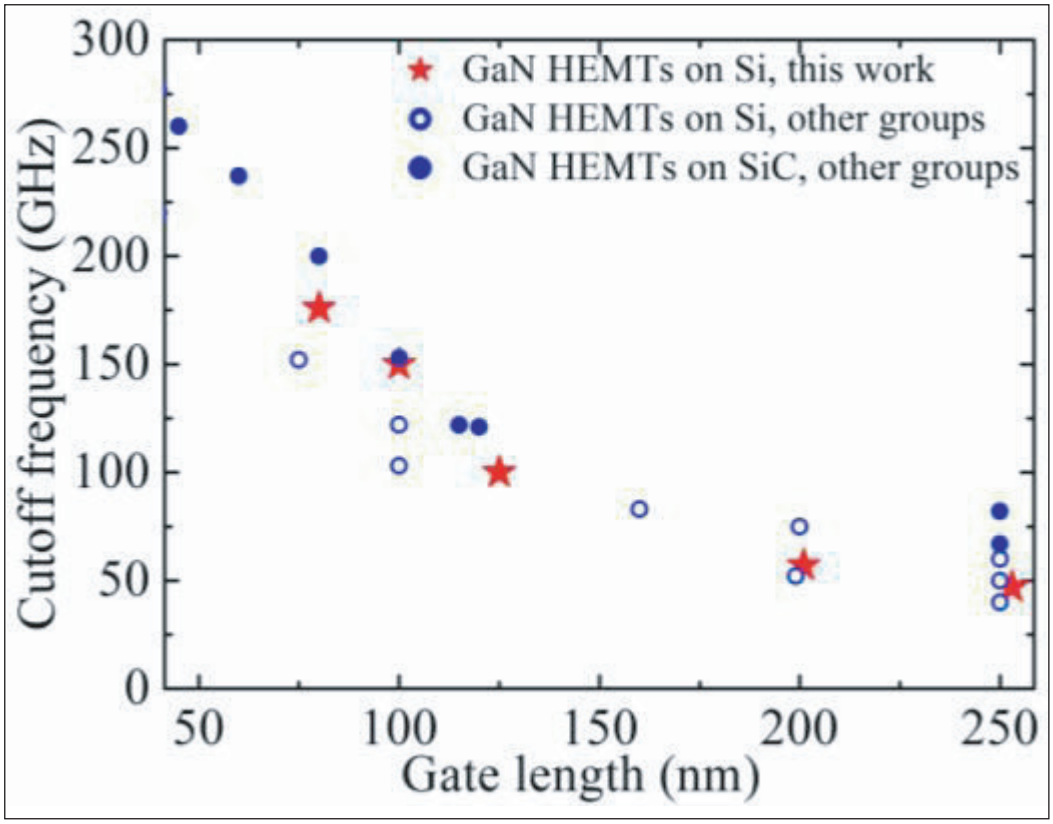

Figure 2. Comparison of cutoff frequencies of GaN HEMTs on Si with AlGaN barrier design A with best data reported by other groups for GaN HEMTs on Si and on SiC.

The researchers comment: "We ascribe the low contact resistivity to the conversion of Ti into TiN causing the formation of nitrogen vacancies in the barrier layer which lead to a high doping level of the AlGaN underneath the contact."

The team carried out a number of characterizations on a 100nm-gate-length device (Table 2). The researchers attribute the improved performance of design A HEMTs to reduced alloy scattering due to the AlN spacer layer.

RF measurements were carried out between 0.1GHz and 50GHz. Using extrapolations and de-embedding corrections, the cut-off frequency (f_T) for an 80nm-gate HEMT at 20V drain bias and −2.75 gate potential was estimated to be 176GHz. The maximum oscillation frequency (f_{max}) was 70GHz. The low f_{max} was blamed on the simple rectangular gates and low-resistance substrate that was used. "Significant improvements of fmax can be expected by using mushroom gates with reduced gate resistance and high-resistivity substrates", the team writes.

By contrast, the best 80nm-gate $Al_{0.35}Ga_{0.65}N$/GaN HEMTs demonstrated a poor f_T of only 115GHz at 20V drain voltage. HEMTs on SiC can achieve f_T values of 200GHz with a 75nm gate length. The corresponding value for GaN HEMTs on silicon is 152GHz.

Comparing their results with those of others (Figure 1), the researchers comment: "It can be seen that our 80nm-gate HEMT shows competitive f_T performance compared to GaN HEMTs on Si (with Au-based and Au-free contacts) reported by other groups. Moreover, our GaN HEMTs on Si with barrier design A rival successfully the best reported GaN HEMTs on SiC substrates in the 80–125nm gate length range." ■

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Table 2. Results of DC and RF characterization of 100nm-gate HEMTs. DC measurements at 10V drain–source voltage (V_{DS}): maximum drain current (I_D) and peak transconductance (g_m). On resistance (R_{on}) measured at low drain voltage with zero gate potential. Also shown are contact resistance (R_C), sheet resistance (R_S), specific contact resistance (ρ_C), and cut-off frequencies (f_T) at 10V and 20V V_{DS} (−2.75V gate potential).

Barrier design	I_D	g_m	R_{on}	R_C	R_S	ρ_C	f_T at 10V	f_T at 20V
A	1.13A/mm	388mS/mm	0.9Ω-mm	0.13Ω-mm	169Ω/sq	1x10^{-6}Ω-cm^2	115GHz	150GHz
B	0.95A/mm	360mS/mm	1.6Ω-mm	0.6Ω-mm	365Ω/sq	1x10^{-5}Ω-cm^2	79GHz	107GHz