Silicon monoxide passivation for gallium nitride transistors

Researchers in China and UK achieve improved subthreshold, Schottky and breakdown characteristics for GaN-based HEMT transistors.

Shandong University in China and University of Manchester in the UK have reported room-temperature thermal-evaporation silicon monoxide (SiO) passivation for aluminium gallium nitride (AlGaN) barrier high-electron-mobility transistors (HEMTs) [Gengchang Zhu et al, Appl. Phys. Lett., vol109, p113503, 2016].

The passivation reduced leakage currents and increased breakdown voltages compared with unpassivated and silicon nitride (SiN_x) passivated devices. The researchers comment: "Because of the good passivation effectiveness, no ion damage, simple preparation technology, and low cost, the thermally evaporated SiO is a promising candidate as a surface passivation for GaN-based HEMTs, especially for high-power and noise-sensitive applications."

The SiNx passivation reference was produced using 300°C plasma-enhanced chemical vapor deposition (PECVD), which can suffer from ion damage. "Compared with PECVD and other techniques, thermal evaporation has many advantages such as no ion damage, technical simplicity, and low cost," the researchers claim.

Although the team mentions avoiding current collapse under pulsed current operation as a motivation for passivation, the paper does not report any measurements that would be needed to assess that effect.

SiO has a higher dielectric constant of 5.0 compared with silicon dioxide's 3.9. The breakdown field of both these silicon oxides is around 10MV/cm. Although thermally evaporated SiO has been assessed for use with other technologies such as thin-film transistors, the researchers say that very little work has been carried out on its use in GaN HEMT passivation.

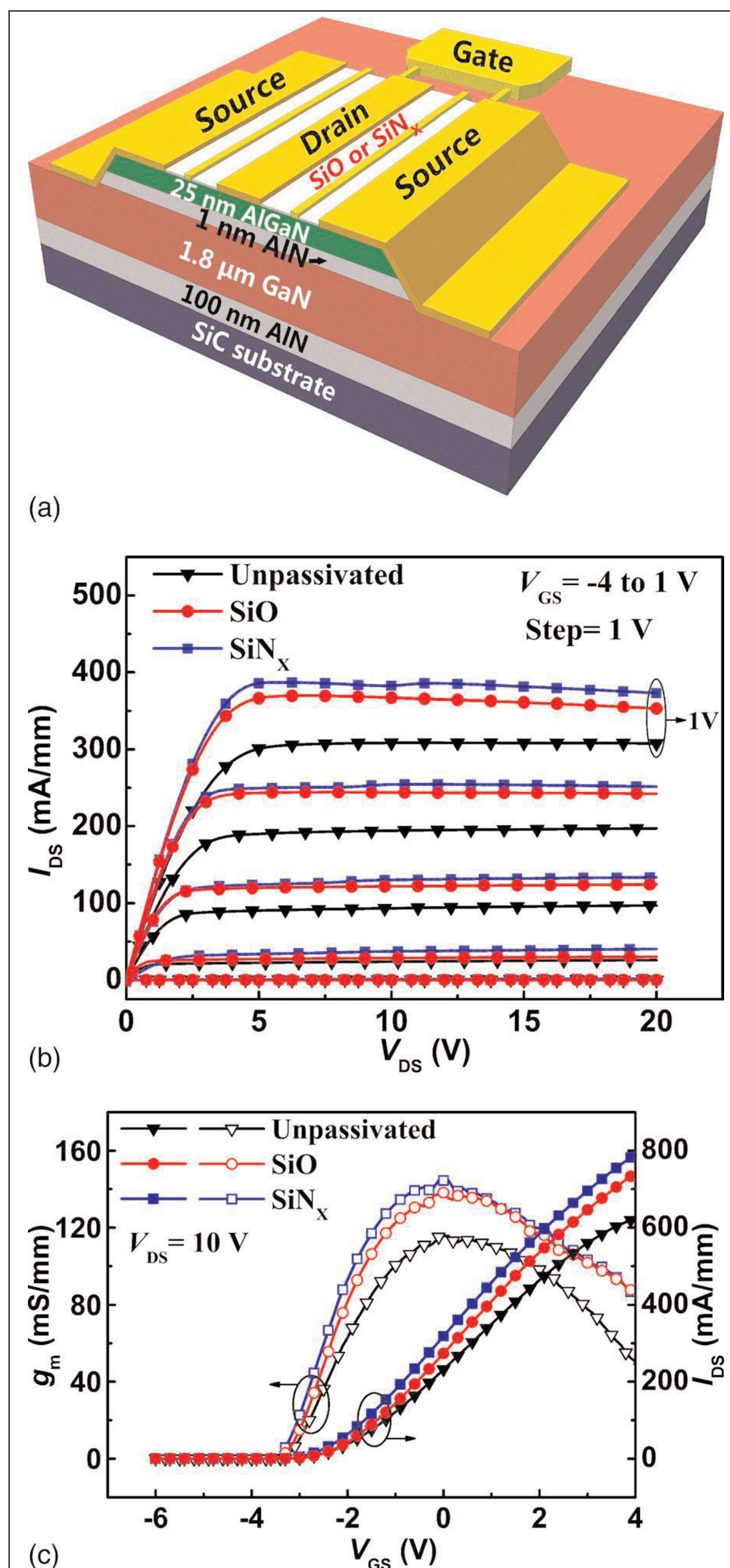

Figure 1. (a) Schematic cross-section of the AlGaN/AlN/GaN HEMTs. (b) Output and (c) transfer characteristics of the unpassivated, SiO-passivated, and SiN_x-passivated AlGaN/AlN/GaN HEMTs.

The device material was grown on 6H polytype silicon carbide (SiC), using metal-organic chemical vapor deposition (Figure 1). The conducting two-dimensional electron gas (2DEG) near the GaN/barrier interface had $1.05 \times 10^{13}/cm^2$ sheet carrier density, 298Ω/square sheet resistance, and $18^{10}cm^2/V$-s carrier mobility (μ_n), according to Hall measurements.

Device fabrication created plasma-etch mesa isolation, annealed/alloyed titanium/aluminium/nickel/gold source–drain ohmic contacts, nickel/gold gate, 100nm SiO passivation, and plasma-etch contact-pad opening.

The placing of the 2μm-long gate in the 13μm source–drain gap gave a gate–drain distance of 6μm. The gate width was 100μm.

Passivation with SiO, and the SiN_x reference, increased Hall sheet carrier density but reduced mobility (Table 1). The researchers suggest that the reduction in mobility could be related to increased Coulomb scattering due to the increased carrier density. The product of carrier density and mobility is higher for the passivated samples. The SiN_x has a marginally higher product than SiO passivation.

The performance in terms of maximum drain current (I_{Dmax}) and transconductance (g_m) at 10V drain bias (V_{DS}) on the HEMTs is again better for the passivated devices, with SiN_x passivation giving better results. The current and transconductance improvements were, respectively, 19% and 18% for SiO, and 25% and 24% for SiN_x. The researchers attribute the improvement to the increased carrier density-mobility product.

However, the SiO passivation has subthreshold and Schottky characteristics that significantly improve on both the unpassivated and SiN_x-passivated devices — that is, lower off-current (I_{off}), higher on/off current ratio (I_{on}/I_{off}), lower subthreshold swing (SS), lower gate leakage (I_g), and higher Schottky barrier height (Φ_B). The SiO passivation also gives the lowest ideality factor (n) for the Schottky diode gate.

The interface trap density (D_{it}) is also lower for SiO passivation. The researchers comment: "The increased density of interface traps for the SiN_x-passivated HEMTs is probably caused by the ion bombardment during the PECVD process, which can be avoided by applying the thermally evaporated SiO."

Table 1. Summary of measurements.

Sample	Unpassivated	SiO	SiN_x
n_s [$10^{13}/cm^2$]	1.05	1.25	369
μ_n [cm^2/V-s]	1810	1.32	385
I_{Dmax} [mA/mm]	309	1760	137
g_m [mS/mm] @ V_{DS} = 10V	116	1690	144
I_{off} [mA/mm] @ V_{GS} = −5V	2.0×10^{-3}	2.1×10^{-4}	3.0×10^{-1}
I_{on}/I_{off}	1.5×10^5	1.8×10^6	1.3×10^3
SS [mV/decade]	181	95	447
D_{it} [$10^{12}/cm^2$-eV]	3.76	1.16	11.30
I_g [mA/mm] @ V_{GS} = −5V	3.3×10^{-3}	3.3×10^{-4}	4.1×10^{-2}
n	1.77	1.75	1.83
Φ_B [eV]	0.79	0.85	0.73
V_b [V] @ V_{GS} = −5V	175	206	111
f_T [GHz] @ V_{DS} = 10V, V_{GS} = 0V	4.0	5.2	5.8

Another improvement of SiO passivation is for breakdown voltage (V_b) with −5V gate (V_{GS}), giving the 'off' state. Breakdown was defined at 10^{-4}A drain leakage. The breakdown current was set at a level that did not destroy the devices. The high V_b is claimed to be the result of lower gate leakage and off-current for the SiO passivation.

The SiN_x passivation gives a higher current-gain cut-off (f_T), while the performance of the SiO-passivated HEMT is better than the unpassivated device. In other studies, SiN_x passivation has variously improved and degraded f_T performance. The researchers comment: "The increase of f_T for the SiO-passivated and the SiN_x-passivated HEMTs is attributed to the increased g_m and decreased overall capacitance of C_{GD} and C_{GS}." ■

http://dx.doi.org/10.1063/1.4962894

Author: Mike Cooke

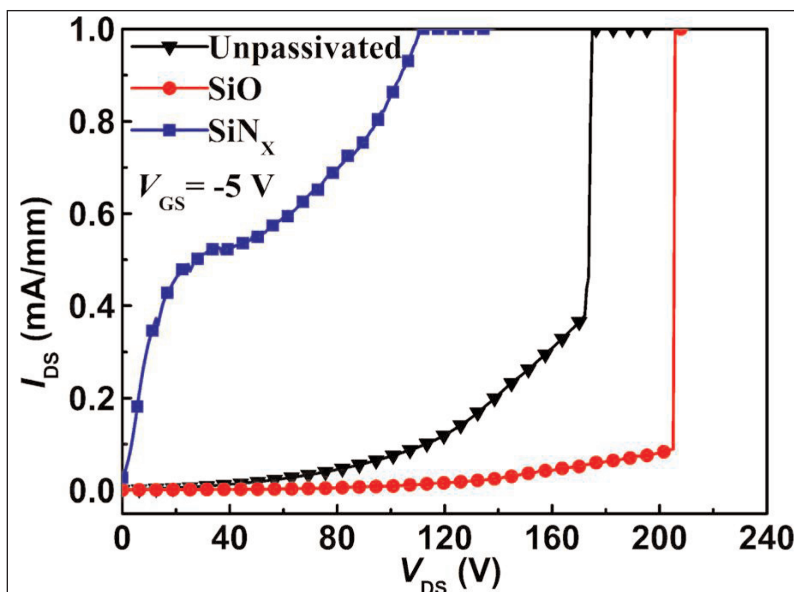

Figure 2. Off-state breakdown characteristics of unpassivated, SiO-passivated, and SiN_x-passivated AlGaN/AlN/GaN HEMTs.