GaN-on-silicon platform for low-cost high-power electronics

Mike Cooke reports on recent research towards devices for high-voltage and high-frequency power switching and RF wireless transmission amplification.

An interesting recent feature of gallium nitride (GaN) electronic development is the use of silicon substrates, often in the form of commercial epitaxial wafers from suppliers like China-based Enkris Semiconductor or Japan's NTT Advanced Technology Corp. It is almost understood that, to compete on cost, the devices will need to be deployed on silicon, and many research papers now do not even bother rehearsing the reasons or challenges. The main reasons are low material costs and availability of large-diameter wafers for mass production. Challenges include higher defect levels arising from mismatches in terms of the crystal lattices and thermal expansion of silicon and III-N materials.

GaN high-electron-mobility transistors (HEMTs), also known as heterostructure field-effect transistors (HFETs), are being developed for high-voltage, high-density, high-frequency power switching and radio-frequency (RF) wireless transmission amplification. Normally-on or 'enhancement-mode' (E-mode) transistors are particularly sought for reduced power consumption and enabling fail-safe high-voltage power switching operation. Also, the normally-off mode simplifies gate-driver circuit design. The high voltage and power handling is based on GaN's high critical electric field before breakdown.

The predominant n-channel devices that have been developed largely depend on the creation of 'two-dimensional electron gas' (2DEG) channels, which arise near the interface between GaN and a barrier layer, often aluminium gallium nitride (AlGaN). The 2DEG occurs due to band-bending effects arising from contrasts in the charge distribution in the chemical bonds holding the Ga, Al and N atoms together. Without special measures, the 2DEG channel conducts when the gate potential is 0V, giving a normally-on 'depletion-mode' (D-mode).

Here, we look at recent developments using the GaN/Si platform.

Dual-layer silicon nitride threshold engineering

Researchers in China, Hong Kong, USA and Canada have used two silicon nitride (SiN_x) layers on GaN HEMTs to push the threshold 1V in the positive direction, while reducing off-state leakage and maintaining on-current [Wei-Chih Cheng et al, Semicond. Sci. Technol., vol35, p045010, 2020]. The dual-layer SiN_x acts as a stressor, depleting the 2DEG channel under the gate, and as passivation to reduce off-state leakage through the AlGaN barrier layer. Although the presented devices were all normally-on, more positive threshold voltage (V_{th}) could eventually lead to normally-off transistors.

The team involved researchers from China's Southern University of Science and Technology (SUSTech), Hong Kong University of Science and Technology (HKUST–Washington State University in the USA, University of British Columbia in Canada, GaN Device Engineering Technology Research Center of Guangdong, China, and China's Key Laboratory of the Third Generation Semi-conductor.

The epitaxial material used for the transistors was grown by metal-organic chemical vapor deposition (MOCVD) on 6-inch-diameter <111> Si at Enkris Semiconductor. The devices (Figure 1) were electrically isolated using inductively coupled plasma (ICP) mesa etching. Annealed titanium/aluminium/titanium/gold (Ti/Al/TI/Au) formed the ohmic source-drain contacts. The gate consisted of patterned nickel/gold (Ni/Au).

The two layers of SiN_x were deposited using dual-frequency plasma-enhanced CVD (PECVD). The low-stress passivation layer has an unintentional tensile stress of 0.3GPa. The layer used a process avoiding the low-frequency plasma excitation step, to reduce surface damage from nitrogen ion bombardment. The addition of low-frequency plasma excitation for the second layer produced a high-compressive-stress −1GPa film.

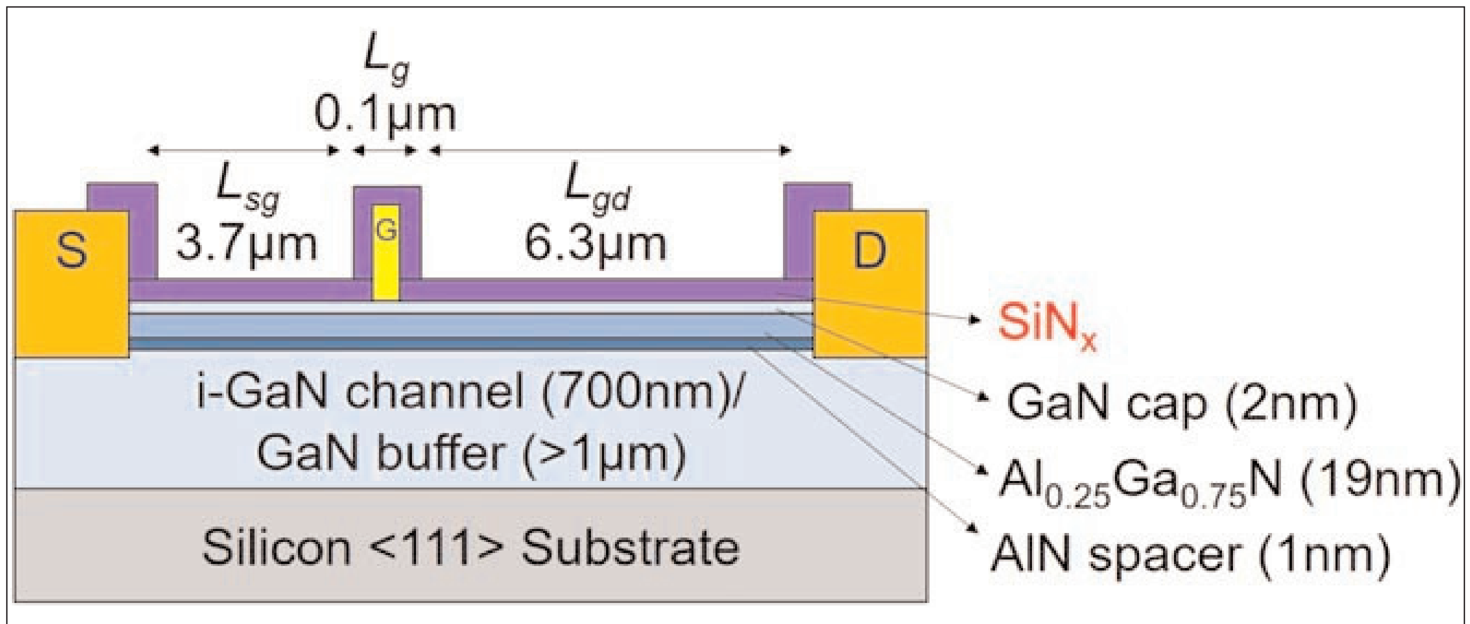

Figure 1. Device structure of AlGaN/GaN HEMT showing gate (L_g), source-to-gate (L_{sg}), and gate-to-drain (L_{gd}) lengths/spacings. Channel consisted of unintentionally doped GaN (i-GaN).

The presence of 200nm stressed SiN_x enabled the V_{th} to be pushed 1V in the positive direction. Combining the stressor with a 14nm passivation layer increased the on-current to the level of a baseline (BSL) device, which had a 200nm SiN_x passivation layer without stressor.

The combined 200nm/14nm stressor/passivation transistor achieved a maximum on-current of 1A/mm (Figure 2). The peak transconductance was 280mS/mm with 7V drain bias, putting the device in the saturation region. The drain current was comparable with the baseline transistor, while the transconductance was higher by around 30mS/mm.

RF measurements gave a cut-off (f_T) of 36GHz, while the stressed device without passivation only achieved 20GHz. The BSL component had a comparable f_T of around 36GHz.

Surface damage also adversely affected the off-current (I_{off}) in the stressed devices without passivation. Adding passivation thicker than 7nm reduced the off-current leakage even below that of the baseline device.

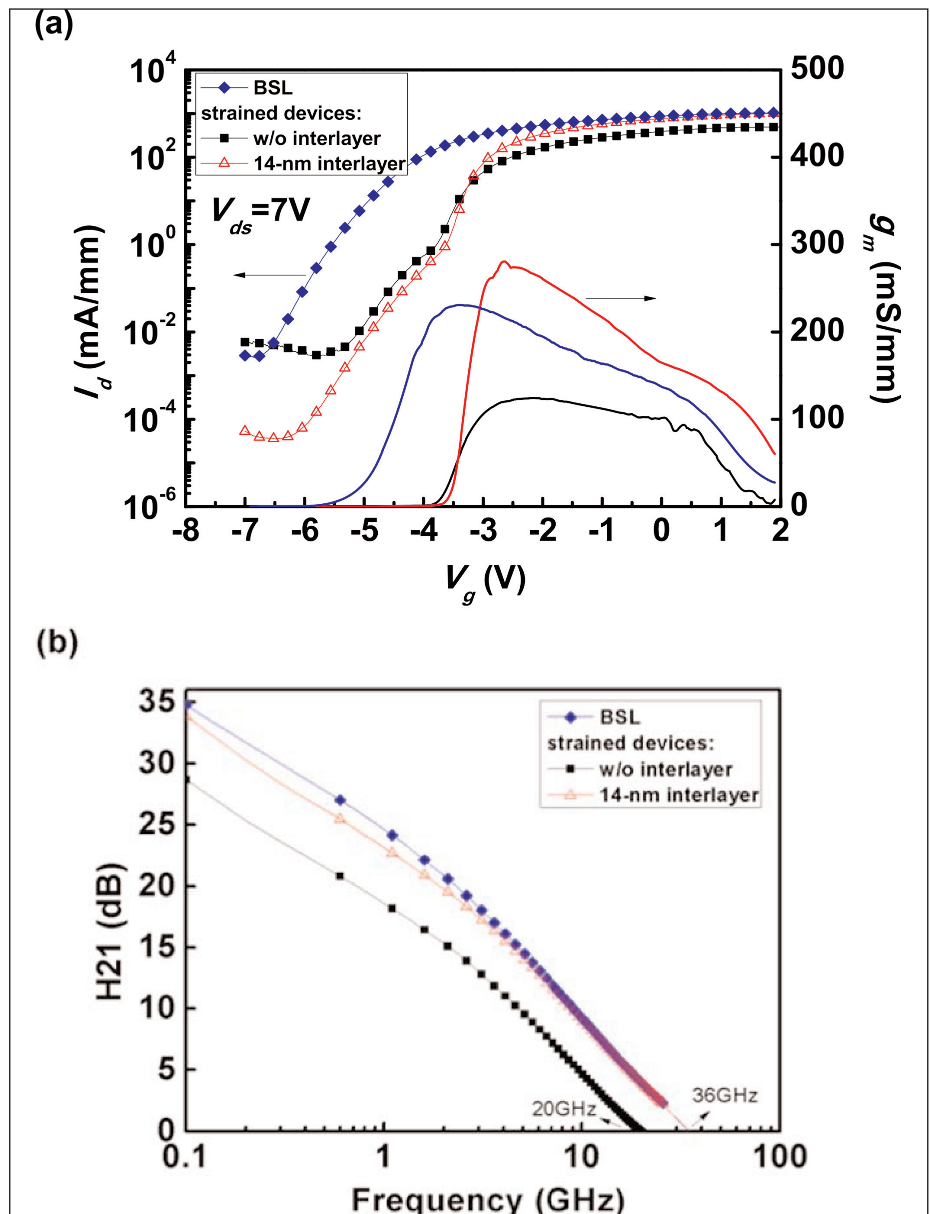

Figure 2. (a) Transfer characteristics of BSL and strained devices at 7V drain bias. (b) H_{21} current gain of BSL and strained devices biased to 7V drain and 1V above gate threshold.

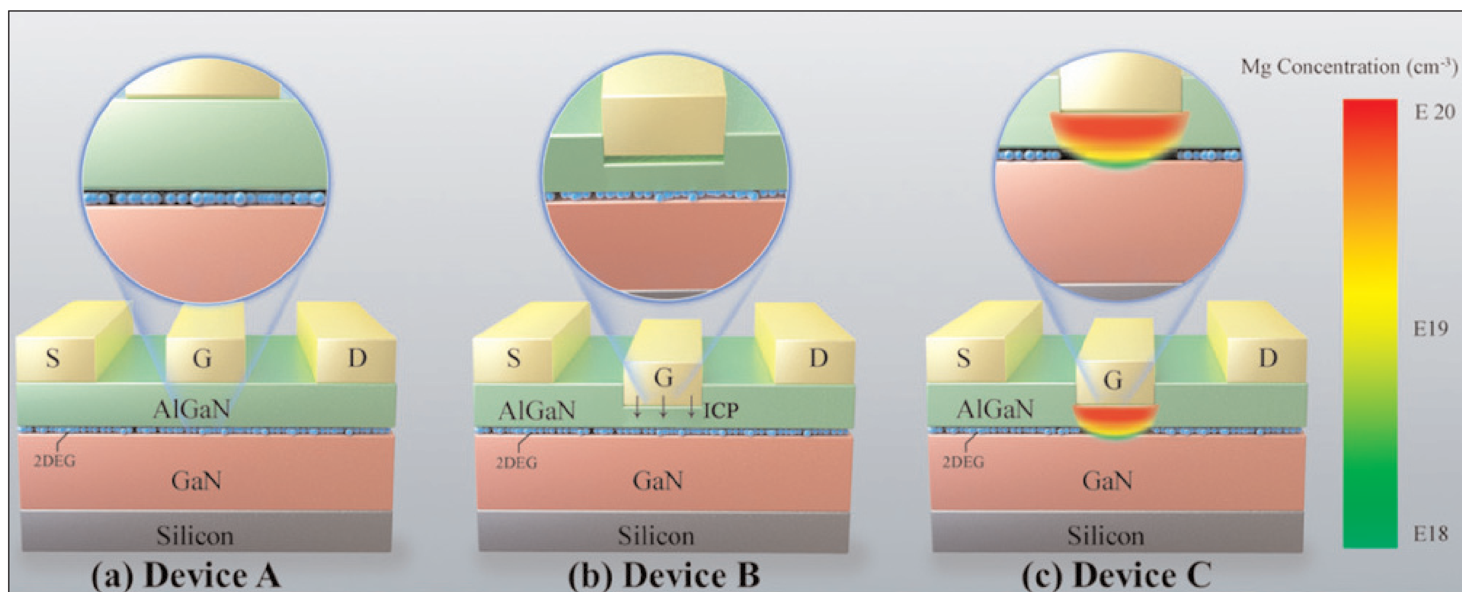

Figure 3. Schematics of (a) bare-bones as-grown device A, (b) device B with etched recessed gate, and (c) device C with Mg diffused gate stack after etching treatment.

Magnesium thermal diffusion for p-gates

South China University of Technology has developed a simplified fabrication process for normally-off AlGaN-barrier GaN-channel HEMTs with a p-type gate stack [Lijun Wan et al, Appl. Phys. Lett., vol116, p023504, 2020]. Introducing p-type material above the channel in the gate region of the device is one technique for depleting the 2DEG, cutting off current flow at 0V gate potential.

The p-type doping under the gate electrode was achieved by magnesium (Mg) thermal diffusion rather than the more usual inclusion as a precursor in the epitaxial material growth process. The team sees their work as "commercially promising" for manufacture of normally-off HEMTs with low gate leakage. The method successfully increased the Vth into positive values, creating a normally-off device.

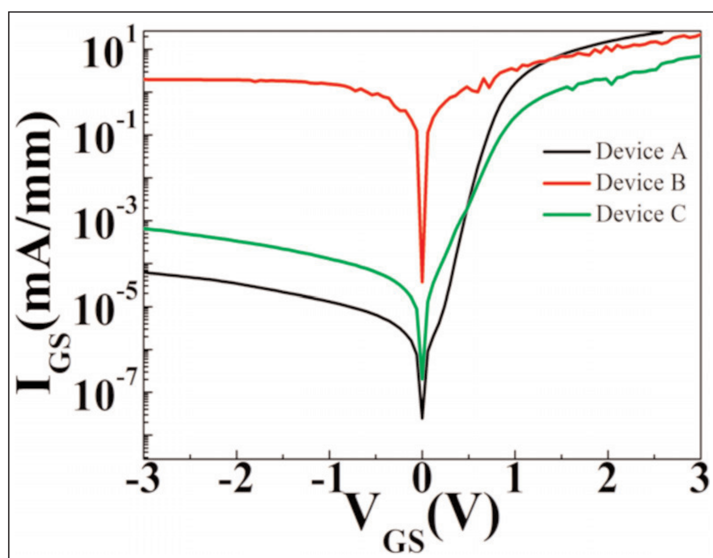

Figure 4. Gate current density (I_{GS}) as function of voltage (V_{GS}) for devices A–C.

The device was based on epitaxial material with 4.7μm buffer, 300nm undoped GaN channel, 15nm $Al_{0.15}Ga_{0.85}N$ barrier, 2nm GaN cap layers on silicon. The transistor fabrication began with 5 seconds of ICP etch in the gate region, before depositing a 50nm layer of Mg with electron-beam evaporation. The underlying AlGaN was p-type doped with the Mg by rapid thermal annealing at 600ºC for a minute. Further annealing in air at 250ºC for a minute created a magnesium oxide (MgO) passivation layer.

The source-drain ohmic contacts consisted of annealed Ti/Al/Ni/Au. Mesa etching with ICP formed the electrical isolation of the devices. A Ni/Au gate electrode on the MgO completed the transistor.

The rapid ICP etch before Mg deposition roughens the surface and introduces defects, allowing the metal atoms to penetrate/diffuse more deeply into the AlGaN barrier layer in the gate region during the thermal anneal. Atomic force microscopy (AFM) suggested that the etch depth was around 6nm, removing the GaN cap and partially etching and recessing the AlGaN.

Three device types were tested (Figure 3): A was a conventional HEMT without ICP etch or Mg diffusion; B was a HEMT with ICP etch, recessing the gate, but no Mg in the gate region; and, finally, C had the full gate stack with ICP etch and Mg diffusion.

The V_{th} for transistors A-C, in order, were −1.5V, −0.4V and +1.4V. The corresponding peak transconductances were 68mS/mm, 105mS/mm and 97mS/mm. Although the gate control, as represented by the peak transconductance, fell back somewhat for device C, the value was still higher than for the bare-bones HEMT A.

The process did hit the drain saturation current from 275mA/mm and 300mA/mm for devices A and B, respectively, with C only managing 173mA/mm. The gate potential in these measurements was +3V. The

researchers suggest a depleted 2DEG may be caused by holes injected from the Mg-diffused layer.

The gate leakage currents with 0V gate were $3.7x10^{-5}$mA/mm and $2x10^{-7}$mA/mm for devices B and C, respectively (Figure 4). Transistor C still had only $6.5x10^{-4}$mA/mm gate leakage with the gate at +0.4V. The researchers credit the passivating effect of MgO on surface trap states from the etch processing for the good performance.

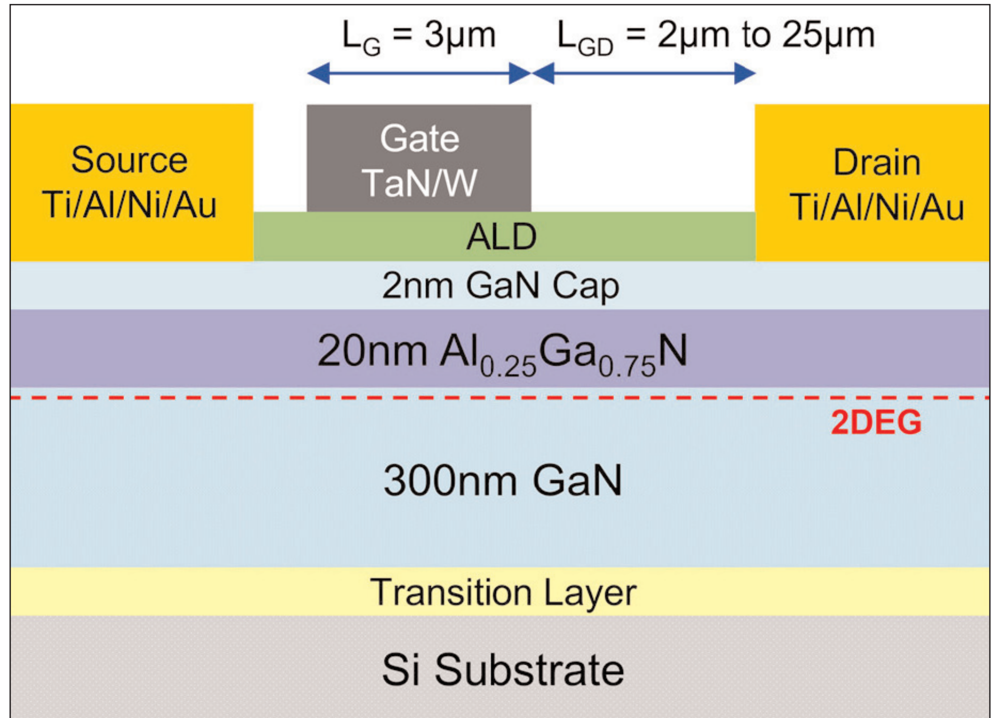

Figure 5. Schematic cross section of AlGaN/GaN MOS-HFET.

Ozone precursor for hafnium dioxide dielectric

North Carolina State University in the USA has been studying ozone (O_3) as means to improve hafnium dioxide (HfO_2) dielectric deposition for AlGaN-barrier insulated-gate metal-oxide-semiconductor HFETs (MOS-HFETs) on silicon substrate [Faisal Azam et al, IEEE Transactions on Electron Devices, vol.67, p881, 2020].

The researchers used AlGaN/GaN epitaxial material on <111> Si, supplied by Japan's NTT Advanced Technology Corp. The device was fabricated using a single dielectric for both gate insulation and surface passivation of the source/drain access regions, much simplifying the processing (Figure 5).

The fabrication sequence was: mesa reactive-ion etch (RIE), deposition and annealing of Ti/Al/Ni/Au source–drain electrodes, ultrasonic and wet surface cleaning of gate and access regions, atomic layer deposition (ALD) of hafnium dioxide (HfO_2) gate/passivation dielectric, post-deposition annealing in nitrogen, and RF sputtering of tantalum nitride/tungsten (TaN/W) gate electrode.

The HfO_2 atomic layer deposition process used tetrakis(dimethylamino)hafnium (TDMAH) as the Hf precursor. For the oxygen component, the team studied the benefits of ozone (O_3) over the more usual water (H_2O). In capacitance-voltage measurements at 10kHz on MOS structures, the effect of using O_3 was to reduce threshold hysteresis by about a factor of two. The team attributes the improvement to reduced charge trapping in defects and possible O_3 AlGaN surface passivation and enhanced interface quality.

The use of O_3 oxidation also tended to shift the threshold from around −12V, for H_2O precursor, to −6V, depending on ALD process details. This might be related to H^+ ions, i.e. protons, being incorporated in the AlGaN surface. Such an effect was absent with O_3.

The researchers also varied the ALD process, alternating the HF precursor with either a single- or double-pulse of oxidant. The single-pulse resulted in a slightly higher capacitance above threshold, compared with the double O_3–O_3 pulse ALD recipe. The researchers suggest that this could be due to variation in thickness of the dielectric layer, or change in dielectric constant with the degree of crystallinity.

The MOS-HFETs reached 340mA/mm maximum saturation drain current with O_3 dielectric, compared with 240mA/mm for H_2O oxidation. The gate potential was 4V. The higher value for O_3 dielectric was attributed to a cleaner HfO_2/AlGaN interface with less surface states affecting the 2DEG conduction channel.

The specific on-resistance with the gate at 3V over pinch-off was reduced by 20% from using O_3 oxidation in a device with 15μm gate–drain distance. "This is a significant enhancement in the performance that should directly translate to lower conduction loss, i.e. higher efficiency in power switching applications," the team writes.

The V_{th} for devices with H_2O, O_3 and no (i.e. a Schottky HFET) dielectric were −12.1V, −4.7V and −2.95V, respectively. The more negative threshold for H_2O dielectric is again blamed on proton incorporation in the AlGaN barrier.

The O_3 oxidant also benefited transconductance, giving a peak value of 112.6mS/mm, compared with 81.38mS/mm for H_2O-based dielectric. Gate leakage was also reduced by more than an order of magnitude by using an O_3 ALD process: $5.4x10^{-6}$A/cm^2, compared with $1.7x10^{-4}$A/cm^2 when H_2O oxidant was used. Studies of the effect of temperatures up to 200ºC on device performance also showed greater stability of on-resistance and V_{th} in the O_3 ALD devices. ➤

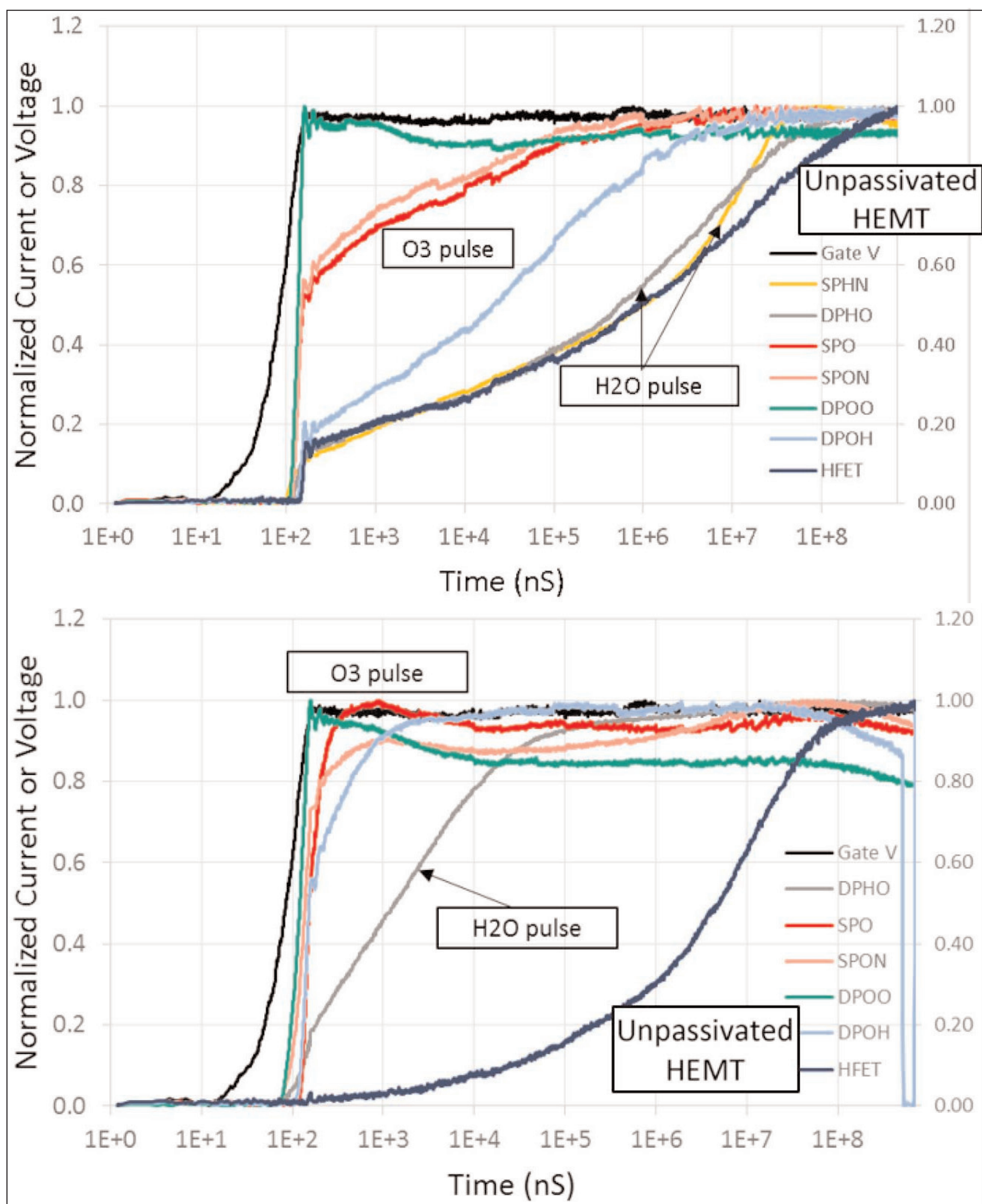

Figure 6. DC/RF dispersion: gate lag at (a) room temperature and (b) elevated temperature, 150ºC.

High-temperature reverse-bias stress testing was carried out for 1000s at 150ºC with 150V drain bias and the gate at 3V below threshold. The H_2O transistors showed a +2.5V drift in threshold (V_{th}) over the test period. The O_3 dielectric reduced this to less than 0.5V.

The current collapse recovery was assessed by applying short pulses with 100ns rise time (Figure 6). The O_3 devices performed significantly better than H_2O or bare Schottky HFETs. "Specifically, H_2O oxidant took 20ms to achieve 90% drain current recovery, whereas O_3 oxidant took ~0.1ms to achieve 90% drain current recovery, an extraordinary 200x potential improvement," the team reports.

The reduced current collapse of the O_3 and H_2O oxidant devices, compared with the unpassivated Schottky HFET, was maintained at 150ºC high temperature. Indeed, the passivated devices showed reduced current collapse, while the Schottky HFET's performance worsened further. Devices where the O_3 was applied in two pulses between the Hf pulse in the ALD process showed "near-ideal behavior", according to the researchers.

Complementary p-channel transistors

Hong Kong University of Science and Technology (HKUST) report on p-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) produced on GaN-on-Si substrates [Zheyang Zheng et al, IEEE Electron Device Letters, vol.41, p26, 2020]. The researchers used commercial 8-inch-diameter GaN-on-Si wafers with epitaxial structures designed for 650V normally-off p-GaN gate power HEMTs (Figure 7).

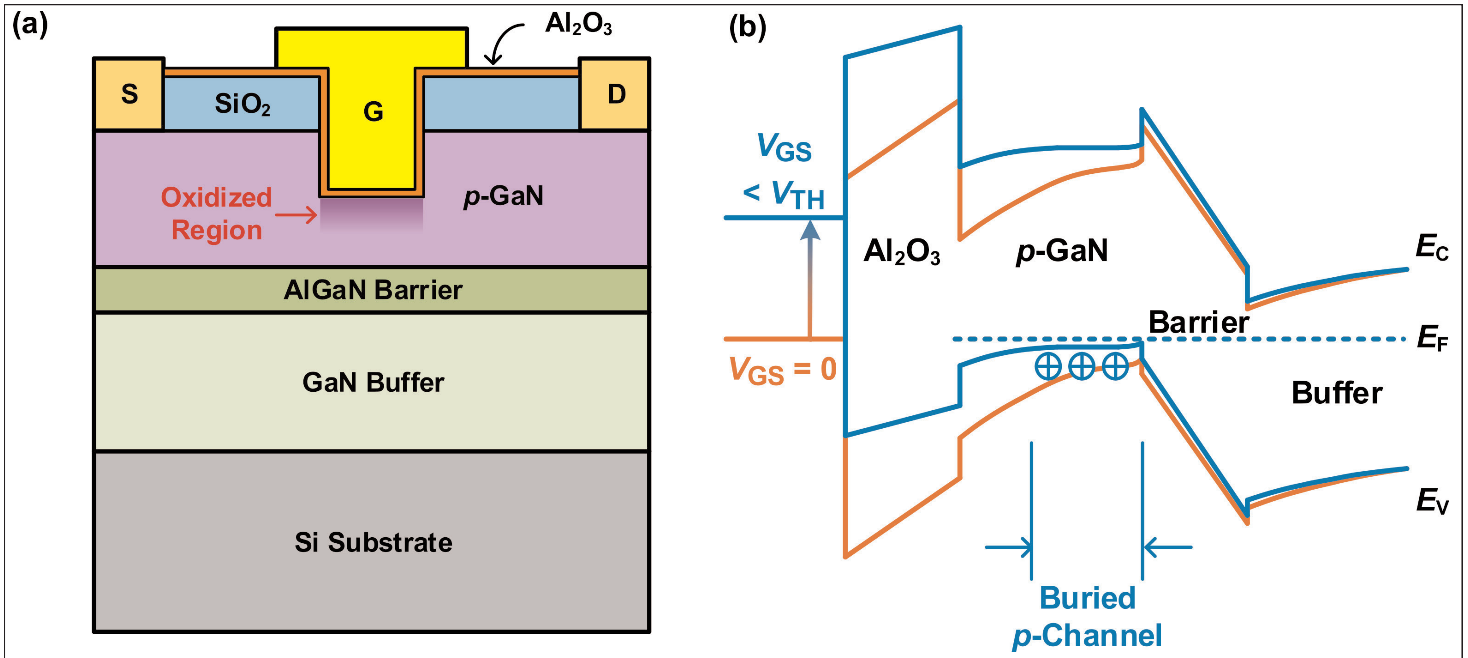

Figure 7. Schematic of (a) E-mode GaN pFET ($L_{GS}/L_G/L_{GD}$ = 4/2/4μm) and (b) energy band diagram at gated region of buried p-channel with 0V (OFF) and beyond threshold (ON) gate potentials (V_{GS}).

As has been seen above, devices with n-type channels with negatively charge carriers (electrons) have been intensively developed in recent years, but the creation of p-channels would enable complementary integrated circuit (IC) designs, which would further reduce power loss in logic control systems. Although some progress has recently been made in developing an analogous two-dimensional hole gas (2DHG) for p-channels, effective devices remain to be achieved. The HKUST work focuses instead on using p-GaN material achieved using magnesium doping.

The GaN-on-Si material included ~12nm AlGaN barrier and ~85nm p-GaN top layer. The undoped GaN buffer was ~4.5μm thick. The structure was found to have a hole sheet density of $1.23 \times 10^{13}/cm^2$ and mobility $10.2 cm^2/V$-s, according to Hall measurements.

The HKUST p-channel devices were fabricated with 500°C-annealed Ni/Au ohmic source–drain contacts evaporated onto the p-GaN, which had previously been subjected to a 5-minute buffered oxide etch, presumably to improve the surface and remove contaminants. The gate recess was defined by a 200nm PECVD silicon dioxide (SiO_2) hard mask, which

Affinity	Platform	V_{TH} [a] (V)	$\lg(I_{ON}/I_{OFF})$ [b]	I_{ON} [c] (mA/mm)	SS (mV/dec)
Notre Dame [10]	p-/i-GaN /AlN Al_2O_3 MOS gate	0.89 (−80 V)	3 (−80 V)	3.87 (−80 V)	1415
RWTH [9]	p-/i-GaN/AlInGaN/ GaN/AlN, Schottky gate	−1.12 (−8V)	7 (−8V)	6.79 (−8V)	91.3
AIST [5]	p-/i-GaN/AlGaN/GaN Al_2O_3 MOS gate	> 4	N.A.	4.00	N.A.
RWTH [11]	p-/i-GaN/AlInGaN/ GaN/AlN, Schottky gate	−0.5	8	1.81	77
HRL [6]	p-/i-GaN/AlGaN/GaN AlN/SiN_x MIS gate	−0.36 (−0.1V)	6 (−0.1V)	1.65	304
AIST [7]	p-/i-GaN/AlGaN/GaN SiO_2 MOS gate	−0.75	3	0.09	817
Cornell [12]	p-/i-GaN/AlN SiO_2 MOS gate	1.32	4	9.10	1027
MIT [13]	p-GaN/AlGaN/GaN Al_2O_3 MOS gate	2.60 (−0.5V)	5 (−0.5V)	1.40	399
This work	p-GaN/AlGaN/GaN Al_2O_3 MOS gate	**−1.7**	**7**	**3.38**	**230**

[a] extracted at $|I_D| = 10$ μA/mm and $V_{DS} = -5$ V unless otherwise specified.
[b] (orders of magnitude) with $V_{DS} = -5$ V unless otherwise specified.
[c] at $V_{DS} = -5$ V and with overdriven V_{GS}, unless otherwise specified.

Table 1. Benchmark of p-channel GaN FETs.

also served as surface passivation. The p-GaN recess was formed using ICP RIE.

An oxygen plasma treatment increased the surface roughness at the bottom of the recess from 0.36nm root-mean-square to 0.41nm, according to atomic force microscopy. The recess depth was found to be about 54nm, leaving ~31nm of p-GaN material above the AlGaN barrier for the channel.

The gate structure was completed with 20nm ALD aluminium oxide (Al_2O_3) insulation and 400ºC-annealed Ni/Au metal electrode. The electrical isolation of the devices was from fluorine ion implantation rather than mesa etching. The researchers used fluorine implant to avoid current leakage along rough mesa sidewalls. The implant occurred between the Al_2O_3 and gate metal deposition steps.

The device demonstrated a V_{th} of −1.7V, giving normally-off enhancement-mode behavior at 0V gate. The oxygen plasma treatment enabled the negative threshold — without the treatment, the device became depletion-mode with the threshold at +2.2V. The on-current of the enhancement-mode device was 67% that of the depletion-mode transistor without oxygen plasma treatment.

The on-resistance for the E-mode device was a "relatively large" 2.4kΩ-mm at low drain bias. This reduced somewhat at −5V drain to 1.6kΩ-mm. The maximum drain current was 6.1mA/mm at −10V drain. The off-current with 0V gate was $1.2x10^{-7}$mA/mm. The team sees this low off-current as "delivering an ultra-low static power consumption required in CMOS logic gates."

The researchers compared their device with others previously presented in the scientific literature (Table 1).

Hydrogen-terminated diamond transistors

École polytechnique fédérale de Lausanne (EPFL) and Lake Diamond SA in Switzerland claim the first p-channel hydrogen-terminated diamond transistors (HTDTs) on GaN-on-Si templates that demonstrate high-power device performance comparable with other HTDTs on polycrystalline and even monocrystalline diamond [Reza Soleimanzadeh et al, IEEE Electron Device Letters, vol41, p119, 2020].

The researchers suggest that the integration of p-channel HTDTs with n-channel GaN transistors opens "a pathway for future complementary power switch and logic applications". The diamond layer is also thermally conductive, allowing improved thermal management of GaN devices in high-power-density applications. The team sees the potential for complementary logic operation, gate drivers and complementary power switches in integrated power inverters and converters.

The researchers used an AlGaN GaN-on-Si template as used for the fabrication of n-channel HEMTs. The template was prepared for diamond deposition by applying layers of 30nm SiN and 5nm Si. These layers were designed to protect the template material from the harsh diamond deposition environment, along with enhancing

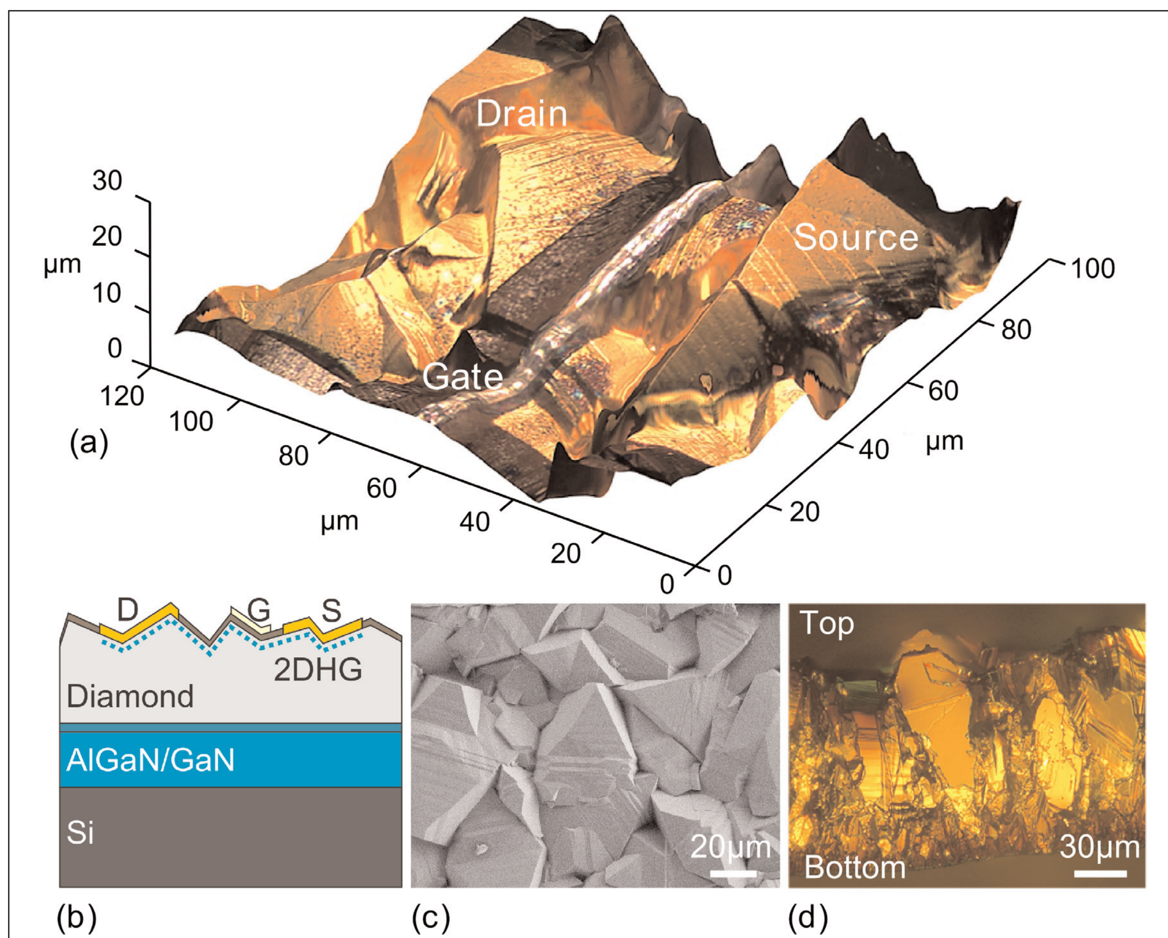

Figure 8. (a) Three-dimensional (3D) optical microscope image of fabricated HTDT, constructed using focus stacking. (b) Schematic of HTDTs. (c) Top-view SEM image of diamond surface. (d) Cross-sectional optical microscope image of diamond layer showing larger grain sizes at top.

adhesion and thermal conductivity between the materials.

The polycrystalline diamond deposition was seeded with 1–150µm nanoparticles applied in isopropanol solution. The main diamond deposition consisted of microwave-plasma CVD (MPCVD) at 800ºC. The plasma power was 3.5kW. The carbon source was 5% methane at 140mbar pressure. Trace quantities of nitrogen and argon were added to improve the growth rate. The carrier gas is not mentioned, but hydrogen is one gas that is used in such processes elsewhere.

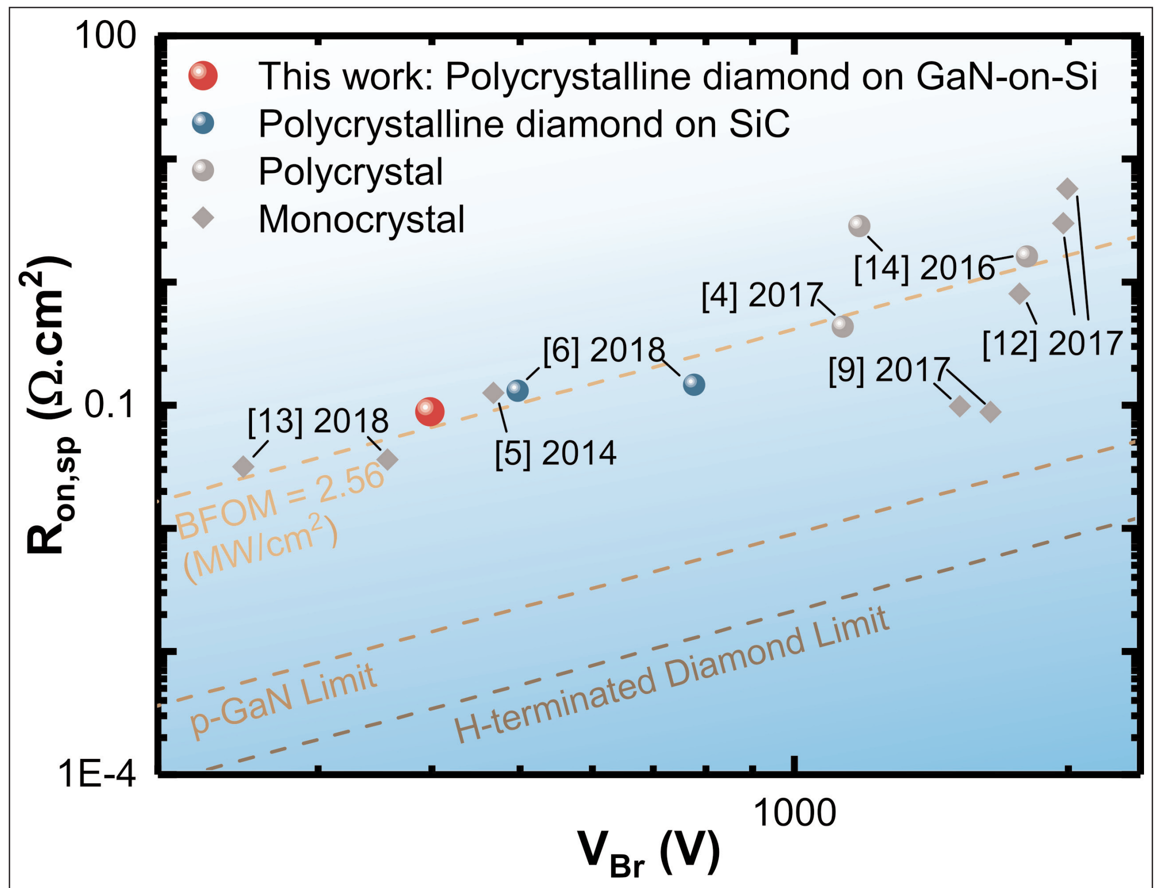

Figure 9. Benchmark of specific-on resistance ($R_{on,sp}$) and breakdown voltage (V_{Br}) of this work with heteroepitaxial material on silicon carbide (SiC), as well as polycrystalline and monocrystalline substrate HTDTs.

Microscopic analysis of the diamond layer showed grains of average size 34µm, smaller than the 100µm grains often reported for the technique. The grains are smaller in the nucleation region, becoming larger at the surface of the 130µm-thick diamond layer.

Further transistor (Figure 8) processing consisted of surface hydrogenation with 650ºC 2.8kW hydrogen plasma, deposition of 200nm-thick Au ohmic contacts, wet-etch Au removal from non-contact areas, 800W oxygen plasma treatment to isolate devices, 200ºC ALD of 80nm aluminium oxide as gate oxide and surface termination, and deposition and plasma-etch patterning of 300nm-thick Al gate electrode.

The hydrogenation resulted in a p-type conductivity with ~10^{14}/cm^2 hole density, according to Hall measurements. The 1.3cm^2/V-s mobility resulted in a sheet resistance of 50Ω/square. The mobility was adversely affected by impurity scattering, the small grain sizes, and the rough surface — values of 3cm^2/V-s have been measured for holes in single-crystal diamond.

The fabricated transistor with 4µm gate length achieved an on/off current ratio of 10^9. The source–gate and gate–drain distances were 2µm and 8µm, respectively. The on-current reached −60mA/mm. The specific on-resistance of 84mΩ-cm^2 is described as "low". The leakage current was "very low" at less than 1µA/mm, even near breakdown.

The breakdown of the device occurred at −400V. The lateral critical field was estimated to be 0.4MV/cm, according to studies using isolated contact pads separated by varying distances. The researchers report that monocrystalline diamond has achieved lateral breakdown fields of 1MV/cm.

The effective lateral thermal conductivity came out at 900W/m-K in samples where the silicon substrate was removed from the backside of the diamond/GaN layers. The diamond grain size in the sample was 3µm on average.

Comparing the performance with other polycrystalline and monocrystalline devices (Figure 9), the researchers observe that "there is still a gap between the performance of current HTDTs and their theoretical limits, which highlights the significant potential for improvement of this technology."

At the same time, the device exceeds the performance of GaN-based p-channel transistors in terms of "6-times higher current density, 4-orders of magnitude higher on-off ratio and more than 6-times higher thermal conductivity". ■

The author Mike Cooke is a freelance technology journalist who has worked in the semiconductor and advanced technology sectors since 1997.