# Vertical gallium nitride moves for power electronics

**Mike Cooke reports on transistor and diode performance enabled by vertical device designs.**

There has been increased reporting of research and development work on gallium nitride (GaN) vertical electronics devices in the past couple of years. Vertical devices offer improved breakdown voltage, current handling and thermal performance in a smaller footprint, compared with more conventional lateral GaN high-electron-mobility transistors (HEMTs), planar metal-oxide-semi-conductor field-effect transistors (MOSFETs) and Schottky barrier diodes (SBDs).



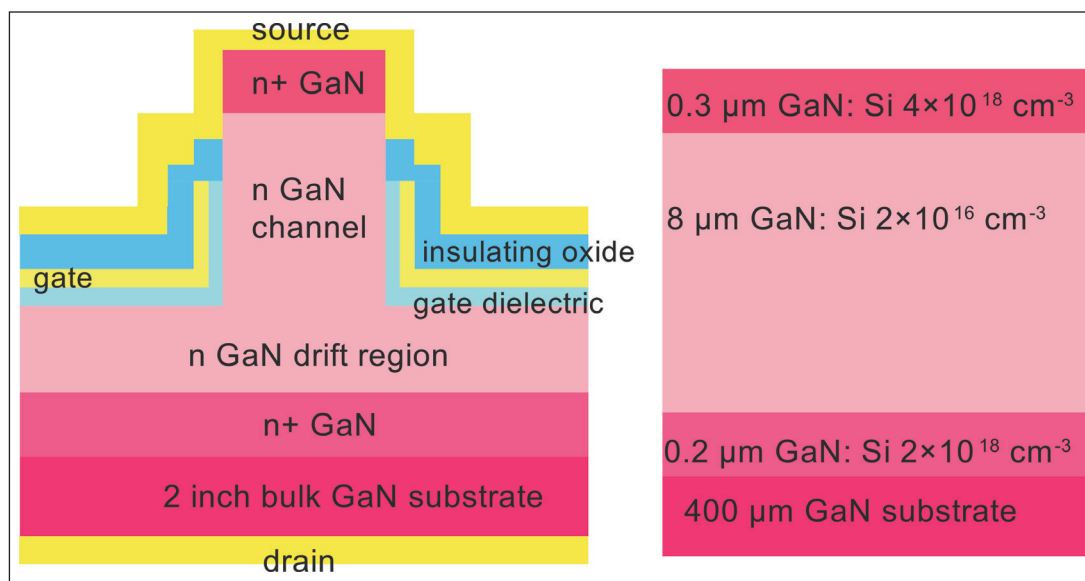Figure 1. Schematic of vertical fin power FET and starting epi-structure.

Vertical devices are mainly fabricated from material grown on expensive free-standing GaN substrates. Despite the cost, such devices should make better use of GaN's material properties such as ultralow conduction loss under high voltage and high temperature than the restriction to lateral devices of GaN grown on foreign substrates such as sapphire, silicon carbide (SiC) or silicon.

Free-standing GaN also has much lower dislocation densities, which is vital for efficient vertical high current conduction and blocking.

Most reports of vertical GaN devices use expensive free-standing substrates, but with increased interest in vertical applications researchers hope material costs will continue to fall in the near future with development. Here, we report on some recent vertical GaN devices, produced mainly, but not exclusively, on free-standing or bulk substrates.

## Fin power FETs

Massachusetts Institute of Technology (MIT) has developed a vertical GaN fin power field-effect transistor (FET) [Min Sun, et al, IEEE Electron Device Letters, online 17 February 2017]. The device structure avoids the use of material re-growth of p-GaN layers. Material re-growth increases process complexity and

(in a manufacturing context) cost. Layers with p-type GaN tend to have high resistance due to the difficulties of magnesium doping.

The MIT researchers are targeting high-voltage, high-current, low-cost, high-performance power electronics applications. The demonstrated fin power FET with suitable electric field engineering techniques achieved an 800V hard breakdown in the off-state with 0V gate potential.

Lateral GaN devices are now commercially available with 650V breakdown. The MIT teams see the advantages of vertical structures as being:
(1) die area does not depend on breakdown voltage;
(2) surface is far from high electric field regions, minimizing trapping effects;
(3) high current levels, thanks to easier current extraction when source and drain contacts are positioned vertically on opposite sides of wafer; and
(4) high thermal performance due to more widely spread current and electric field distribution.

The epitaxial material was grown using metal-organic chemical vapor deposition (MOCVD) on 2-inch bulk GaN (Figure 1). Submicron fins with 70º sidewalls were etched using inductively coupled plasma based on chlorine/boron trichloride chemistry. The dry etch was followed by hot tetramethylammonium hydroxide (TMAH) wet etching to give vertical sidewalls.

Alignment of the fins with the $<11\bar{2}0>$ a-plane of the GaN crystal structure gave smoother fins. The fins were 100mm long and 0.18mm wide.

The gate consisted of 15nm atomic layer deposition (ALD) aluminium oxide dielectric and sputtered molybdenum metal electrode. The metal electrode and dielectric were removed from the tops of the fins. Plasma-enhanced chemical vapor deposition (PECVD) silicon dioxide was used as a spacer to isolate the gate metal from the source electrode. The source and backside drain metals were annealed titanium/aluminium.

The on/off current ratio was as high as $10^{11}$ with a 5V drain bias (Figure 2). The gate leakage was less than $10^{-4}$A/cm$^2$ at a gate-source potential difference of 5V. The threshold voltage for an on/off current ratio of $10^5$ was 1.0V. Based on extrapolation, a higher threshold of 1.5V was found. The researchers comment: "The threshold voltage can shift more positively by reducing the doping density in the channel or scaling down the channel width even further."

The subthreshold swing was as low as 75mV/decade and hysteresis effects were small. The on-resistance was 0.36mΩ-cm$^2$ based on fin area and 3.24mΩ-cm$^2$ based on device area. The low annealing temperature of the source-drain electrodes gave imperfect ohmic behavior.
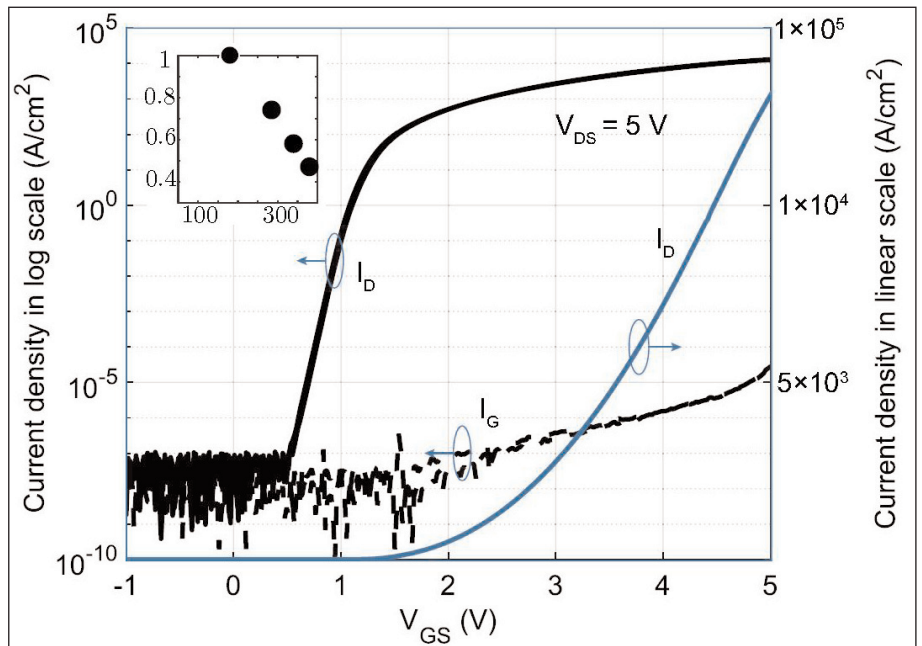
Without edge termination, hard 0V gate off-state breakdown occurred at 100V. A gate field-plate termination structure on silicon dioxide at the device periphery increased breakdown to 400V. "In both cases, the breakdown mechanism is due to gate dielectric failure," the team reports. Further increase in breakdown voltage to 800V was enabled by filling the trenches of the device with 100nm silicon dioxide before gate formation.

The researchers also present a benchmark comparison with the performance of power transistors produced by other groups (Figure 3).

## Junction barrier Schottky diodes

Cornell University, Qorvo Inc and IQE RF LLC in the USA have worked on vertical junction barrier Schottky diodes (JBSDs) produced on freestanding GaN [Wenshen Li, et al, IEEE Transactions on Electron Devices, published online 21 February 2017]. The aim was to combine the good characteristics of SBDs and pn diodes (PNDs) for power applications.

SBDs have low turn-on voltage, but suffer from higher current leakage under reverse bias. By contrast, pn diodes have high turn-on and low reverse-bias leakage. High current under reverse bias reduces the effective breakdown voltage (BV) characteristics of SBDs.



**Figure 2. Double sweep transfer curves of fabricated vertical fin power FET with channel width 180nm: left — y-axis in log scale; right — y-axis in linear scale. Inset: threshold voltage ($V_{th}$ (y-axis, in volts) as function of channel length (x-axis, in nm).**
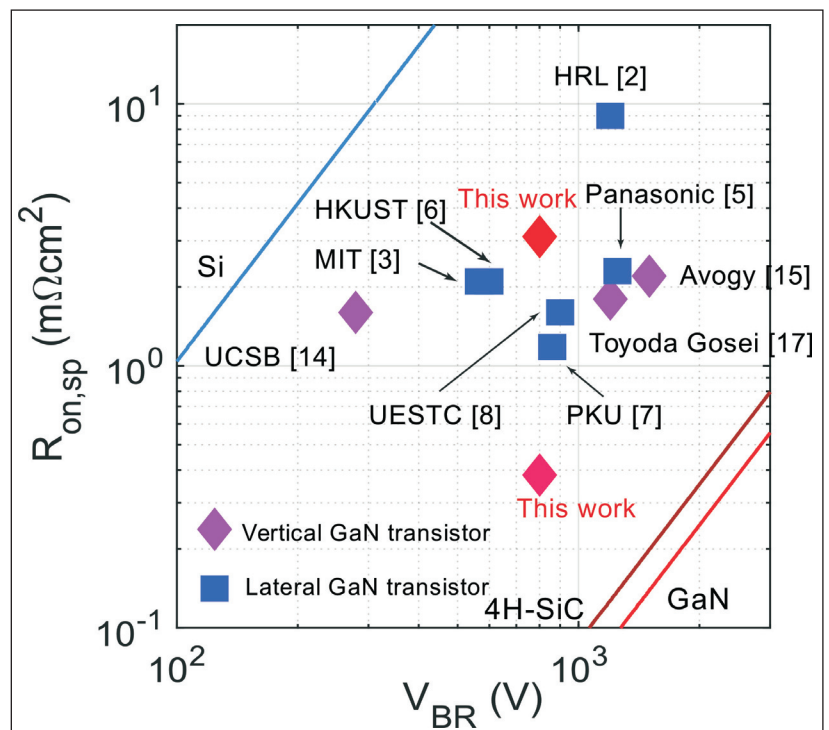


**Figure 3. Specific on-resistance ($R_{on,sp}$) versus breakdown voltage ($V_{BR}$) of GaN vertical fin power FET, along with other normally–off lateral and vertical GaN transistors. Top point averaged by total device area and other point averaged by total fin area.**
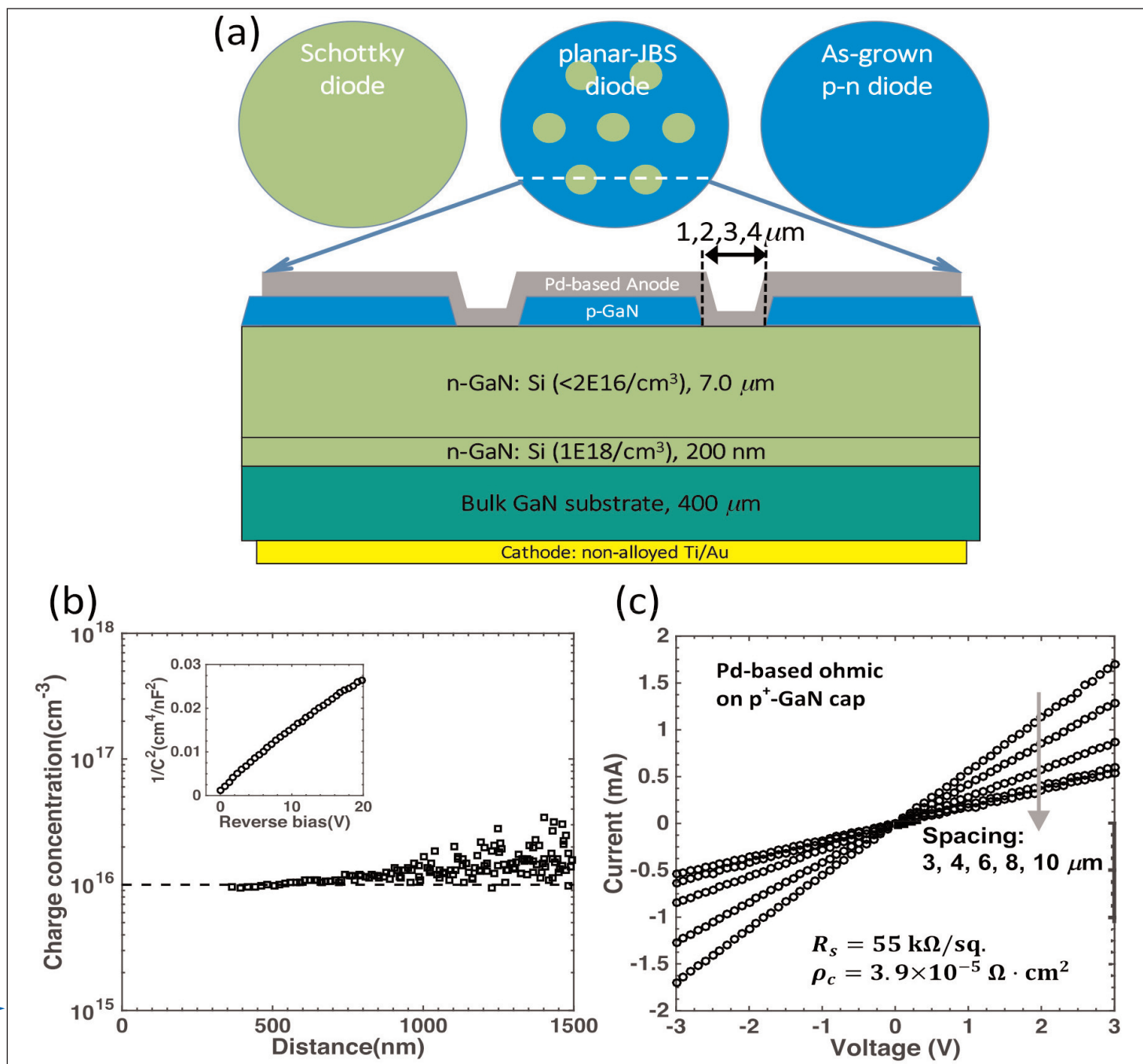
**Figure 4. (a) Schematic device top view and cross section of fabricated trench JBSD. Total Schottky (trench) area is designed to be the same for each trench diameter. (b) Carrier concentration in n-GaN drift layer extracted by capacitance–voltage measurement at 1MHz. (c) Representative transmission line method current–voltage characteristics of Pd-based ohmic contact on p-GaN with calculated sheet resistance ($R_s$) and specific contact resistivity ($\rho_c$).**

By using pn and Schottky barrier structures, the JBSD can combine low turn-on with low reverse-bias leakage through reducing the surface field (RESURF). However, attempts to use lateral pn junctions suffer from increased process complexity from using ion implant or re-growth steps.

Instead, Cornell/Qorvo/IQE used a vertical structure with trenches in p-GaN material reaching down to give Schottky contacts with n-GaN (Figure 4).

The team comments that Panasonic used a similar trench JBSD to give superior breakdown and simul-

taneously low on-resistance in work presented in 2015. Cornell/Qorvo/IQE add: "However, the RESURF effect could not be explicitly confirmed, since the characteristic shift of the turn-on voltage was not observed and the leakage behavior of the diodes was not reported."

MOCVD on free-standing GaN was used to create the semiconductor material of the diodes. The substrate had a threading dislocation density of ~$2\times10^6$/cm$^2$. High dislocation densities lead to higher reverse-bias leakage in general. Non-free-standing GaN substrates such as sapphire and silicon carbide tend to lead to
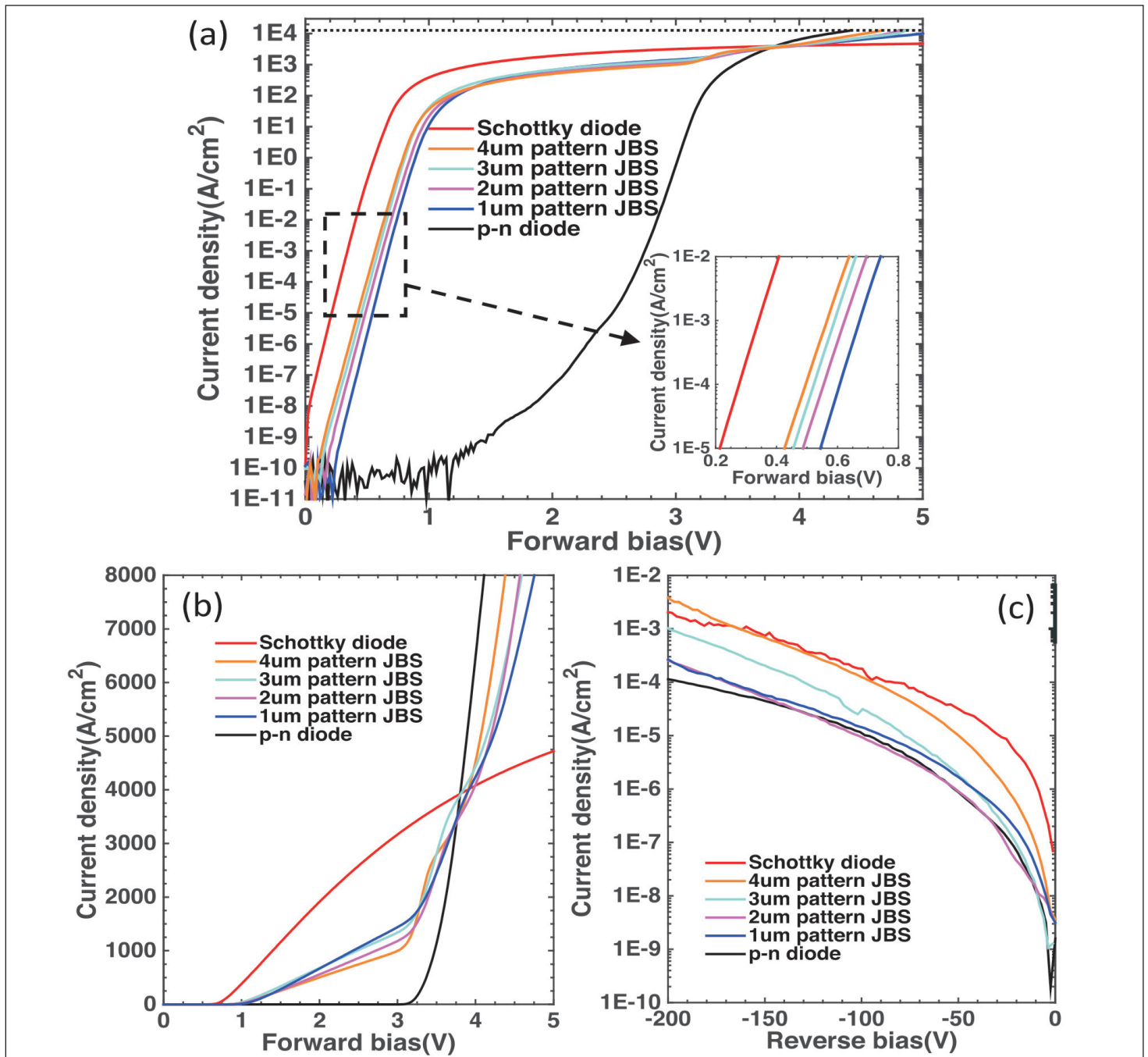
**Figure 5. Measured current-voltage characteristics of trench JBSDs. (a) Forward bias characteristics in log scale. (b) Forward bias in linear scale showing two-step turn-on. (c) Reverse bias in log scale.**

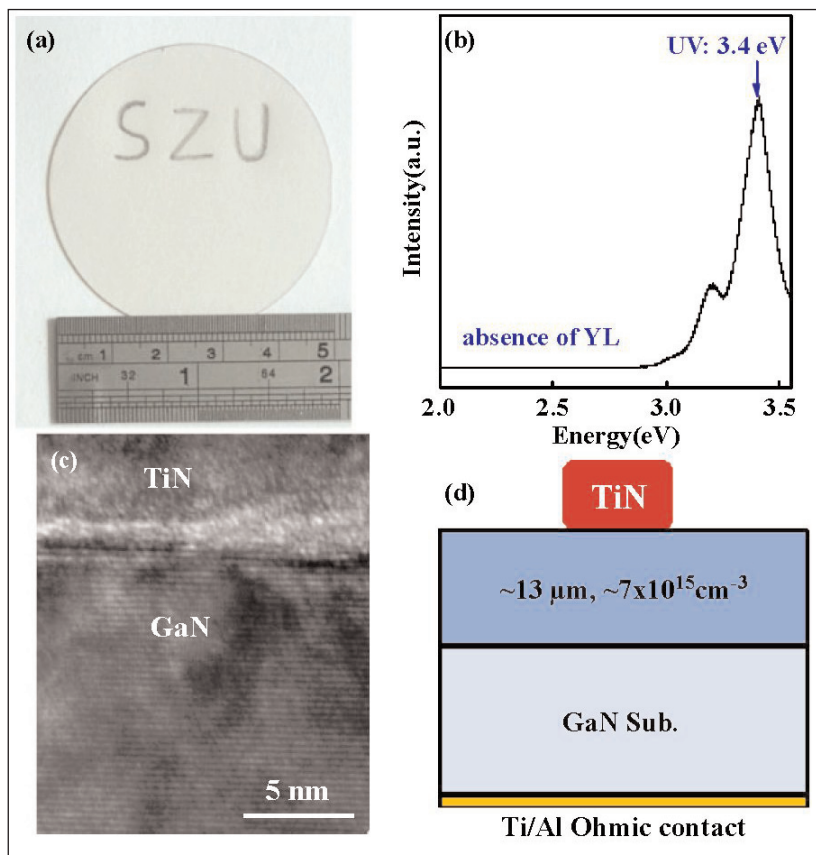higher-dislocation-density GaN epitaxial material due to lattice mismatch.

The trenches for the JBSD structure were formed by dry etching. Circular trenches were chosen since the researchers expected this to result in a more uniform field profile along the periphery, giving a less restricting size constraint compared with striped/linear trenches.

The anode of the diode was palladium-based (Pd-), giving ohmic and Schottky contacts with p-GaN and n-GaN, respectively. The devices were 100mm in diameter. The researchers comment: "No additional field-plate (FP) structures are used for edge termination, since the additional leakage often associated with the FP process might mask the trend in the leakage current

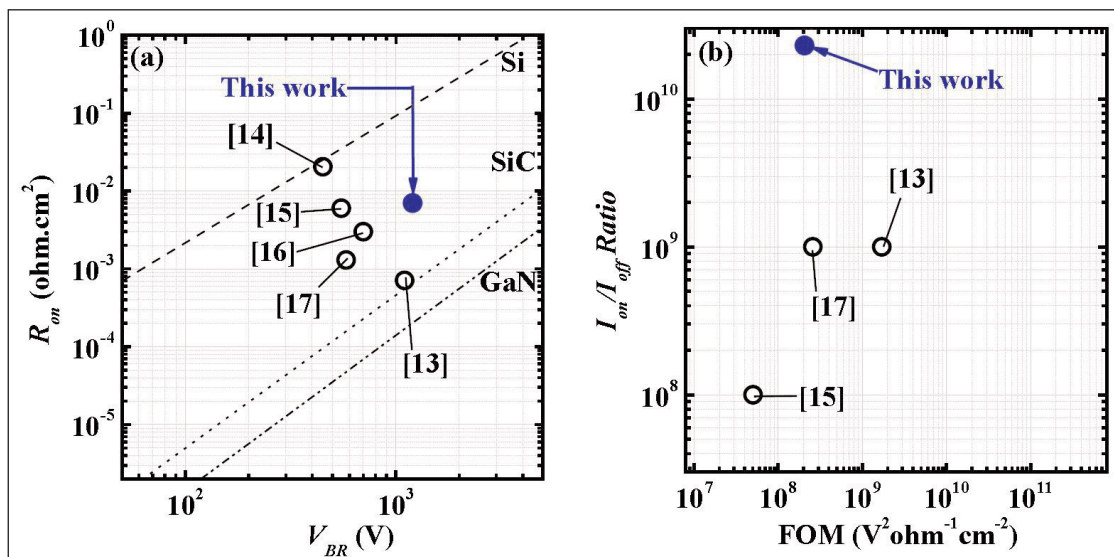of trench JBSDs designed with varied trench sizes."

Simulations with stripe trenches suggested that the surface electric field arising from positive charge under the Schottky contact terminates at the depletion region in the p-GaN instead of the Schottky contact, reducing the surface field's vertical component.

The JBSDs and the comparison SBD turned on with around 1V forward bias and an ideality factor in the range 1–1.05 (Figure 5). The turn on shifts upwards as the trench becomes smaller. Reverse-bias leakage was reduced as the trench size was scaled downwards. "Up to 20 times reduction in leakage current is achieved in the 1mm trench JBSDs compared with conventional SBDs, reaching the pn diode leakage level," the team

**Figure 6. (a) Photograph of free-standing GaN wafer. (b) Room-temperature photoluminescence spectrum of free-standing GaN wafer with strong peak at 3.4eV from near-band-edge ultraviolet transition. (c) Transmission electron microscope cross-section of TiN/GaN stack. (d) Schematic of fabricated vertical GaN SBDs.**

The breakdown voltages of the pn diodes and JBSDs were similar, in the range 250–650V. The SBD breakdown was generally somewhat lower, in the range 275–425V. The SBD performance was probably affected by severe edge field crowding at the anode metal edge. The researchers expect high breakdown voltages with suitable edge termination structures.

The reverse current leakage at 150V bias increased from pure pn diode to Schottky barrier diode, through increasing-trench-size junction barrier Schottky diodes. The pn diode current density leakage was in the range $10^{-5}$–$10^{-4}$A/cm$^2$, while the SBD leakage was spread between $\sim$3x$10^{-4}$A/cm$^2$ up to $\sim$10$^{-1}$A/cm$^2$.

## Gold-free Schottky barrier diodes

Researchers in China and Japan have developed a gold-free Schottky contact for GaN, claiming records for on/off current ratio and breakdown voltage for vertical GaN Schottky barrier diodes [Xinke Liu et al, Jpn. J. Appl. Phys., vol56, p026501, 2017].

The team from Shenzhen University, Shanghai University, Shanghai Institute of Microsystem and Information Technology, and Suzhou Institute of Nano-Tech and Nano-Bionics (SINANO) in China and Tokushima University in Japan believe that such a development could lead to the use of underutilized small-diameter silicon CMOS fabrication facilities. They explain: "In silicon CMOS foundries, gold is typically not used in the front-end process, because gold could cause deep-level traps in silicon, which are the carrier recombination centers that can reduce the carrier lifetime in silicon." Usually, Schottky contacts on GaN use nickel and gold.

"These devices could be generally useful for cost-competitive power switching circuits with a supply voltage in the range of 500–700V," the researchers write.

The 2-inch free-standing (0001) GaN wafer was grown by hydride vapor phase epitaxy (HVPE) with typical defect density $\sim$10$^5$/cm$^2$. The resistivity was about 0.01Ω-cm and the surface roughness was about 0.2nm. A 13mm GaN layer was

reports, adding: "As the total trench area is designed to have the same total area, the reduction in leakage current is due to the RESURF effect arising from the trench JBSD design."



**Figure 7. Open symbols: GaN SBDs with gold; solid symbols: GaN SBDs without gold: (a) V$_{BR}$ versus R$_{on}$ and (b) I$_{on}$/I$_{off}$ ratio versus FOM of fabricated and state-of-the-art GaN SBDs.**

added by MOCVD. The background doping was around $7\times10^{15}/cm^3$. The Hall mobility was measured at $\sim1250cm^2/V\text{-}s$.

The 250mm-diameter circular SBD structure consisted of 100nm of sputtered titanium nitride (TiN) that was etched into an electrode through chlorine-based plasma reactive ion etch (Figure 6). The etch process had a selectivity factor for TiN over GaN of around 100. The back-side contact consisted of alloyed 50nm Ti and 200nm aluminium.

The turn-on voltage of the SBD was around 0.69V. The ideality and Schottky barrier height were 1.1 and 0.92eV, respectively. The saturation current under reverse bias was $1.8\times10^{-12}$A, close to the value of $2.5\times10^{-12}$A expected on the basis of forward bias behavior. The on/off current ratio ($I_{on}/I_{off}$) was $2.3\times10^{10}$ using measurements at +1.6V and −2V.

Hard breakdown ($V_{BR}$) under reverse bias occurred at 1200V. The researchers suggest that the breakdown mechanism could be impact ionization. The power device figure of merit (FOM) $V_{BR}^2/R_{on}$ was $2.1\times10^8V^2/\Omega\text{-}cm^2$, using the specific on-resistance ($R_{on}$) of $7m\Omega\text{-}cm^2$ from the linear region of the current–voltage curve. The team plotted benchmark comparisons of $R_{on}$, $V_{BR}$, $I_{on}/I_{off}$, and FOM (Figure 7).

The researchers comment: "Compared with other reported GaN SBDs, the GaN SBDs in this work fabricated with a gold-free process shows the highest breakdown voltage of 1200V. However, the on-state resistance of the fabricated GaN SBDs in this work is slightly higher, implying that further reduction in non-gold ohmic contact resistance is required."

## Silicon substrate

Massachusetts Institute of Technology has developed quasi- and fully vertical pn GaN diodes on silicon, claiming a number of record performance characteristics [Yuhao Zhang et al, IEEE Electron Device Letters, published online 30 December 2016]. The researchers see possible application of the techniques to include vertical power transistors and advanced rectifiers, leading to competitive low-cost devices for 200–600V power switching.

The MIT researchers estimate silicon wafer costs to be $0.08/cm², which compares with $\sim$2.2/cm² for 4-inch sapphire and $\sim$100/cm² for 2-inch GaN substrates.
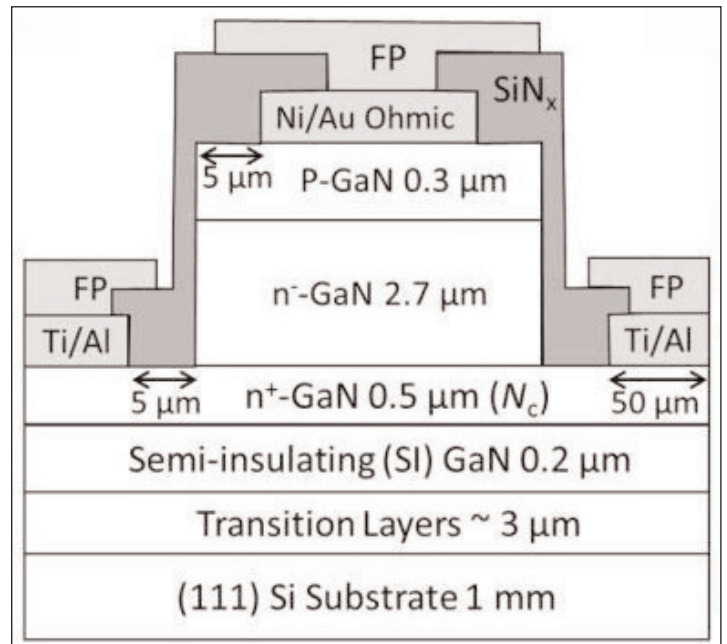


**Figure 8. Quasi-vertical pn diode with passivation and field-plate (FP) structures.**

The III-nitride epitaxy consisted of MOCVD on 2-inch (111) silicon. The transition layers used aluminium gallium nitride (AlGaN) alloys. The semi-insulating GaN was achieved with iron doping. The low-electron-carrier-density n⁻-GaN drift layer used carbon doping with propane precursor.

The quasi-vertical diodes (Figure 8) used deep etch down to the n-GaN cathode layer for mesa isolation and silicon nitride passivation.

For the fully vertical structure (Figure 9), the epitaxial material was flipped and bonded to a (100) silicon substrate. Before bonding, the device mesa-isolation regions were defined by deep etching down to the (111) silicon growth substrate.

The compression bonding was carried out at 300ºC for 20 minutes. A nickel layer protected the (100)
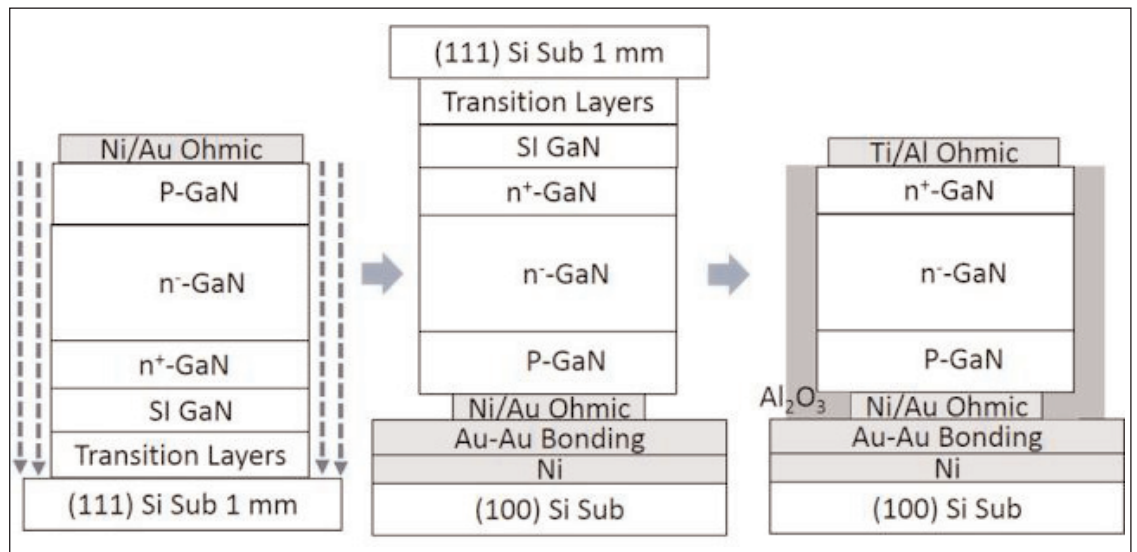


**Figure 9. Fabrication sequence for fully vertical pn diode.**
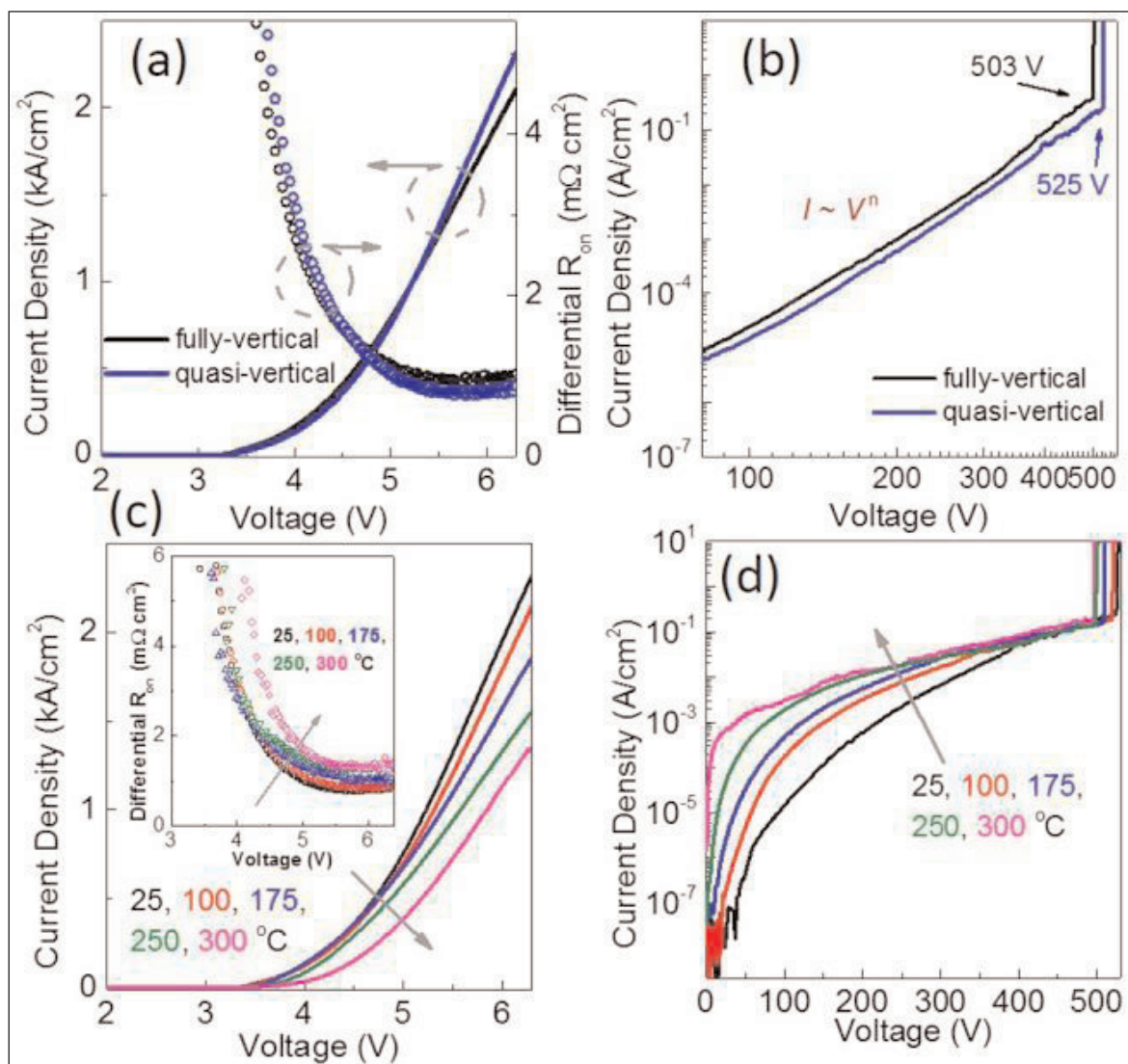
**Figure 10. (a) Forward and (b) reverse characteristics of diodes, along with corresponding (c and d) temperature-dependent measurements.**

The breakdown voltage under reverse bias was more than 500V for both devices. The leakage at 300V reverse bias was about $5 \times 10^{-3}$ A/cm$^2$, and still less than $10^{-2}$ A/cm$^2$ at 400V. These values are two orders of magnitude better than previous GaN-on-Si vertical diodes, according to the team. Further, the leakages are the lowest among all reported GaN vertical diodes on foreign substrates, lower than for lateral GaN diodes, and comparable with commercial SiC diodes, it is claimed.

The peak electric field was estimated to be 2.5–2.6MV/cm. Reference diodes without the carbon-doped n$^-$-GaN layer demonstrated lower breakdown voltage and increased reverse bias leakage. The researchers believe that reducing edge-type dislocations could increase the breakdown to 800V. Even higher values could be achieved with material able to sustain higher peak fields in the 2.8–2.9MV/cm range.

The devices also performed well at increased temperatures up to 300ºC with little degradation of on-resistance. The differential on-resistance at 300ºC was as low as 1.35mΩ-cm$^2$. Improved heat management could be provided by substrate thinning.

The devices also had reverse recovery times (~50ns, for switching from ~400A/cm$^2$ to 200V reverse bias) "comparable to the best reports for GaN-on-GaN diodes". Another claimed record for GaN-on-Si vertical diodes is the Baliga figure of merit (BV$^2$/R$_{on}$) of 0.32GW/cm$^2$. ∎

silicon wafer during the sulfur hexafluoride (SF$_6$) deep plasma etch used to remove the growth substrate. Further etching through the transition layers exposed the n$^+$-GaN contact for subsequent formation of the ohmic contact. ALD aluminium oxide (Al$_2$O$_3$) provided 20nm-thick passivation.

At a forward bias of 5.3V, the differential specific on-resistance was 0.8mΩ-cm$^2$ for the quasi-vertical and 1mΩ-cm$^2$ for the fully vertical diodes (Figure 10). The current density was of the order of kA/cm$^2$. "This high forward current level is comparable to state-of-the-art GaN-on-GaN vertical diodes," the researchers write. The slightly higher differential on-resistance for the fully vertical device is attributed to flow through the silicon substrate and etch-induced defects in the n$^+$-GaN under the top ohmic contact.

The specific on-resistance of the fully vertical diode as a simple voltage/current ratio was 3mΩ-cm$^2$ at 5.5V (so the current density (V/R) was 1.8kA/cm$^2$). This is claimed to be "the best report for all GaN-on-Si vertical diodes".

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