Expanding the potential of hydride vapor phase epitaxy

Researchers see the growth technique as offering lower silicon doping for vertical gallium nitride power device applications. Mike Cooke reports.

Japan's SCIOCS Co Ltd has been developing its hydride vapor phase epitaxy (HVPE) technology and has recently reported with Hosei University its use as an alternative to metal-organic chemical vapor deposition (MOCVD) for creating very lightly doped n-type gallium nitride (GaN) drift layers in vertical power devices. SCIOCS' researchers believe that device-quality smooth as-grown surfaces with good thickness uniformity can be achieved using HVPE that are comparable with the results of MOCVD. Traditionally, HVPE has been seen as a means to grow thick layers relatively quickly, but with a lower structural quality.

In addition, the firm's researchers have used HVPE to create 6mm-thick free-standing GaN crystals with diameters up to 6 inches. This followed on from the company's claim in 2017 of the first controlled growth of thick GaN layers by an HVPE method with sufficiently low carrier concentrations for drift layers in power-device applications.

The name SCIOCS means 'I know compound semiconductors' (Latin 'scio' + 'CS'). "The name SCIOCS represents our company's philosophy that SCIOCS has the deepest understanding of compound semiconductors, and provides the highest-quality compound semiconductor materials," president Masahiko Kobayashi explains on the firm's website.

SCIOCS was founded in 2015 as part of the Sumitomo Chemical Group, bringing in compound semiconductor activities of Hitachi Cable Ltd, dating back to 1971. Indeed, the firm is located in Hitachi city (-shi), Ibaraki prefecture (-ken). In 2017, Sumitomo Chemical's own compound semiconductor activities were merged with those of SCIOCS.

The company produces GaN substrates and epitaxial wafers, using HVPE and MOCVD, that can be used in microwave equipment (cell phones, base stations, radars and wireless LANs) and in optical equipment (laser diodes for Blu-ray/DVD/CD drives, LEDs for general lighting and LCD backlights). Under development are HVPE aluminium nitride (AlN) templates on sapphire for ultraviolet light-emitting diode application, and potassium sodium niobate (KNN, $(K,Na)NbO_3$) as a lead-free alternative to lead zirconate titanate (PZT, $Pb(Zi,Ti)O_3$) for piezoelectric thin films in micro-electro-mechanical systems (MEMS). SCIOCS used to produce gallium arsenide (GaAs) substrates, but this production line and business has been discontinued.

The use of HVPE technology for vertical GaN-on-GaN growth has been another recent development drive at SCIOCS, creating devices aimed at power conversion using the high frequency and high critical field capability of the material.

Vertical diode

Drift layers in vertical power devices extend the distance over which a potential drops, reducing the electric field and hence increasing breakdown voltages. Epitaxial material for the vertical diode developed with Hosei University was grown on 2-inch free-standing silicon-doped n-GaN substrates [Hajime Fujikura et al, Appl. Phys. Express, vol11, p045502, 2018]. The free-standing substrates were prepared using a void-assisted separation method developed by the researchers during 2003–2017 (see below). The threading dislocation density was uniform in the range $(1–3)x10^6/cm^2$.

The new structure combined epitaxial growth by HVPE and MOCVD methods (Figure 1), and was compared with the results of an MOCVD-only process. The MOCVD-only method required a rather complex n-type drift layer structure (Figure 2). The MOCVD re-growth on HVPE material was prepared with a hydrofluoric cleaning process.

The fabrication of the vertical pn diode (PND) involved mesa etching for isolation and deposition of electrodes consisting of palladium/titanium/gold (Pd/Ti/Au) and indium tin oxide (ITO) for the p- and n-contacts, respectively.

The researchers used an HVPE chamber without quartz parts, as developed by SCIOCS last year [see e.g. Hajime Fujikura et al, Jpn. J. Appl. Phys., vol56, p085503, 2017]. Quartz consists of silicon dioxide. Silicon (Si) and oxygen (O) are donor impurities in GaN. The use of HVPE also avoids carbon (C) incorporation, which is a problem with the metal-organic precursors of MOCVD.

In a quartz-based HVPE system unintended silicon impurity concentration can be of the order of $1\text{x}10^{17}/\text{cm}^3$, while oxygen incorporation is of the order $8\text{x}10^{15}/\text{cm}^3$. In their 2017 research, the SCIOCS team found that, by removing quartz from high-temperature areas of the reaction chamber, oxygen and carbon contents were reduced below the detection limit (mid-$10^{15}/\text{cm}^3$) of the secondary-ion mass spectroscopy (SIMS) system used to measure impurity concentrations. Process optimization enabled the researchers to reduce the silicon concentration to below the SIMS detection limit of $5\text{x}10^{14}/\text{cm}^3$. "To the best of our knowledge, this is the purest GaN layer ever reported to date," the researchers commented at the time.

Low-silicon-impurity GaN layers from quartz-free HVPE also have high resistivity of more than $1\text{x}10^9\Omega$-cm. Such high resistivity could be the base for devices built using ion implantation of silicon and magnesium impurity doping, as in mainstream silicon electronics. The mobility of n-GaN layers with $1\text{x}10^{15}/\text{cm}^3$ electron concentration was $1150\text{cm}^2/\text{V-s}$.

For the more recent research on vertical diodes, the use of quartz-free HVPE was found to reduce non-uniform conductivity due to carbon incorporation and uncontrolled silicon impurity concentration in the drift layer. Non-uniformity was detected by studying electroluminescence variations under a microscope.

Carbon incorporation and the resulting compensation effects in MOCVD material is non-uniform due to the presence of macro-steps of the scale of several tens of microns on the growth surface. The absence of carbon in the HVPE drift layer was confirmed by SIMS.

The team comments: "The absence of carbon compensation and in-plane carrier concentration modulation will make it easy to grow power device structures as they are designed, and hence enable the design of devices with performance reaching the material limitations. Additionally, the absence of off-angle-dependent carrier concentration changes will improve the uniformity and reproducibility of device performance, leading to improved yield in mass production of GaN-based power devices, even if off-angle differences exist within given wafers and/or between wafers."

Off-angle variations arise due to wafer bowing.

A hybrid MOCVD/HVPE diode with 200μm diameter achieved a high breakdown of ~2kV and relatively low on-resistance of $2\text{m}\Omega\text{-cm}^2$ (Figure 3). The device did not have a field-plate structure to avoid field concentration effects at electrode edges. There was some leakage at low forward bias and the ideality was around 2 rather than the ~1 ideality achieved in the comparison MOCVD-only structure.

The researchers comment: "This deterioration could be attributed to dominance of the recombination current through defect and/or impurity levels within the bandgap due to the presence of accumulated silicon at the re-grown interface. However, all of these observed characteristics of the present hybrid pn diode were superior to those recently reported for a similar pn diode having an MOCVD-grown drift layer and a p-GaN layer re-grown by molecular beam epitaxy."

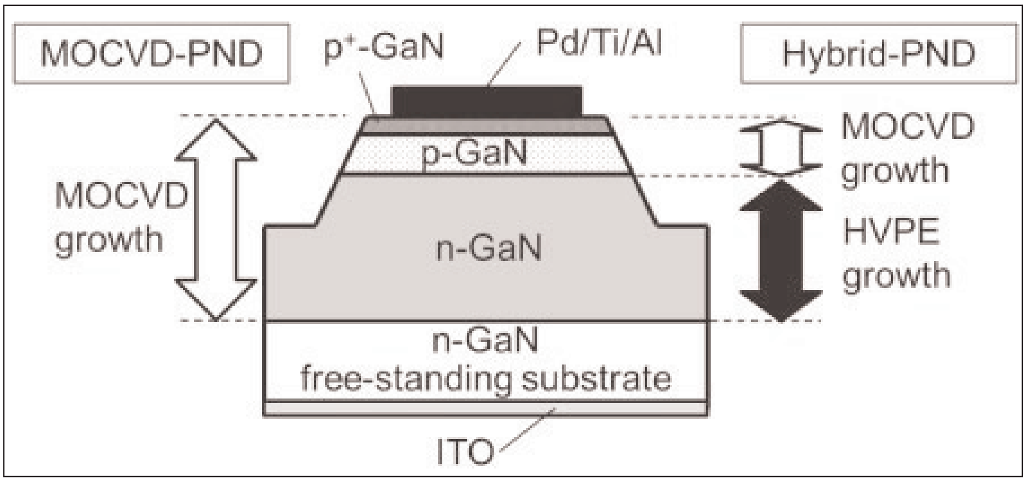

Figure 1. Schematic structure of PN-junction diode.

MOCVD	p-GaN	$2\text{x}10^{20}/\text{cm}^3$ Mg	20nm
MOCVD	p-GaN	$1\text{x}10^{19}/\text{cm}^2$ Mg	100nm
HVPE drift	n-GaN	$2\text{x}10^{15}/\text{cm}^2$ Si	33μm
Substrate	Freestanding n-GaN		

MOCVD	p-GaN	$2\text{x}10^{20}/\text{cm}^3$ Mg	30nm
MOCVD	p-GaN	$1\text{x}10^{19}/\text{cm}^2$ Mg	500nm
MOCVD drift	n-GaN	$1\text{x}10^{15}/\text{cm}^3$ Si	2μm
MOCVD drift	n-GaN	$8\text{x}10^{15}/\text{cm}^3$ Si	15μm
MOCVD drift	n-GaN	$2\text{x}10^{18}/\text{cm}^3$ Si	2μm
Substrate	Freestanding n-GaN		

Figure 2. (Top) HVPE/MOCVD epitaxial structure. (Bottom) MOCVD-only structure.

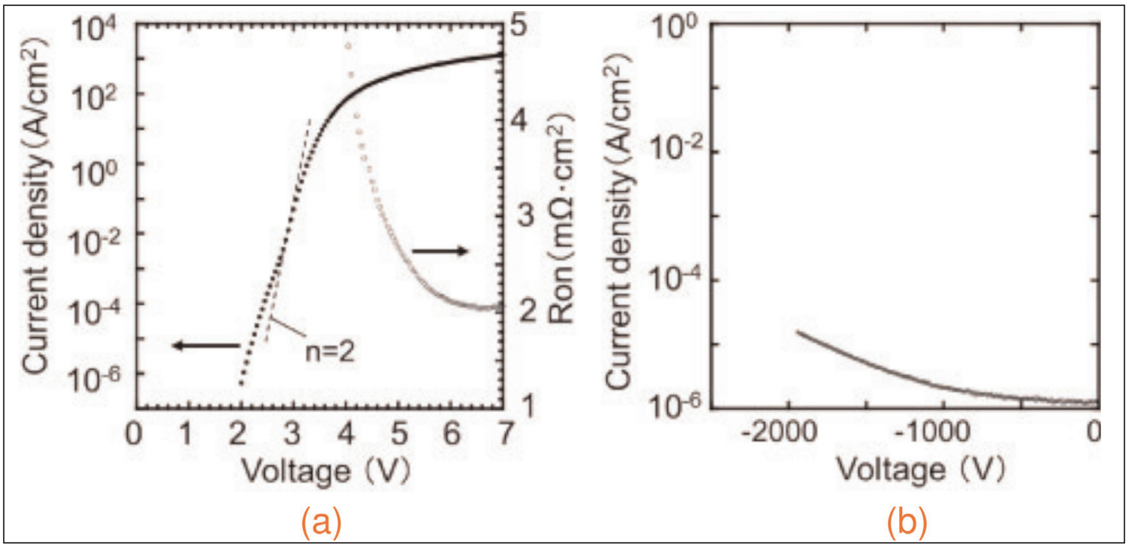

Figure 3. (a) Forward and (b) reverse I–V characteristics of hybrid PN diode made by MOCVD re-growth on HVPE-grown GaN drift layer.

Substrate

SCOICS researchers also used their void-assisted separation method to create 6mm-thick GaN crystals with diameters up to 4 inches [Hajime Fujikura et al, Jpn. J. Appl. Phys., vol57, p065502, 2018]. The team reports that a 6-inch wafer is being processed, but has not yet been characterized: "However, with the availability of similar thick 6-inch bulk crystals as for the 2- and 4-inch crystals, we expect the fabrication of high-quality, macro-defect-free 6-inch GaN wafers from this bulk crystal in the near future."

Void-assisted separation consists mainly of HVPE growth on sapphire (Figure 4). First MOCVD is used to create a thin GaN seed layer with many nanometer-size voids. The HVPE GaN first forms islands on the MOCVD material, which then coalesce and bow the wafer. As the growth proceeds, the bowing becomes less extreme.

The material tends to be less prone to macro-defects, compared with epitaxial layer over-growth methods, since the GaN from the small islands of the seed layer more quickly coalesces. Macro-defects include pits, high-threading-dislocation-density (TDD) regions, inversion domains (IDs), through-holes and cracks.

As the bowing reduces, there are a number of sources of the stress that can lead to cracking. Some stress arises from the bowing reduction. Stress also arises at the edge of the wafer due to increased impurity incorporation compared with the bulk. The edge stress can be reduced by slicing and polishing the final free-standing GaN substrate.

The HVPE process used GaCl as the metal-hydride source. The GaCl was created by flowing hydrogen chloride (HCl) gas over gallium at 800ºC. The nitrogen component of GaN came from ammonia (NH_3). The HVPE growth temperature was typically 1050ºC.

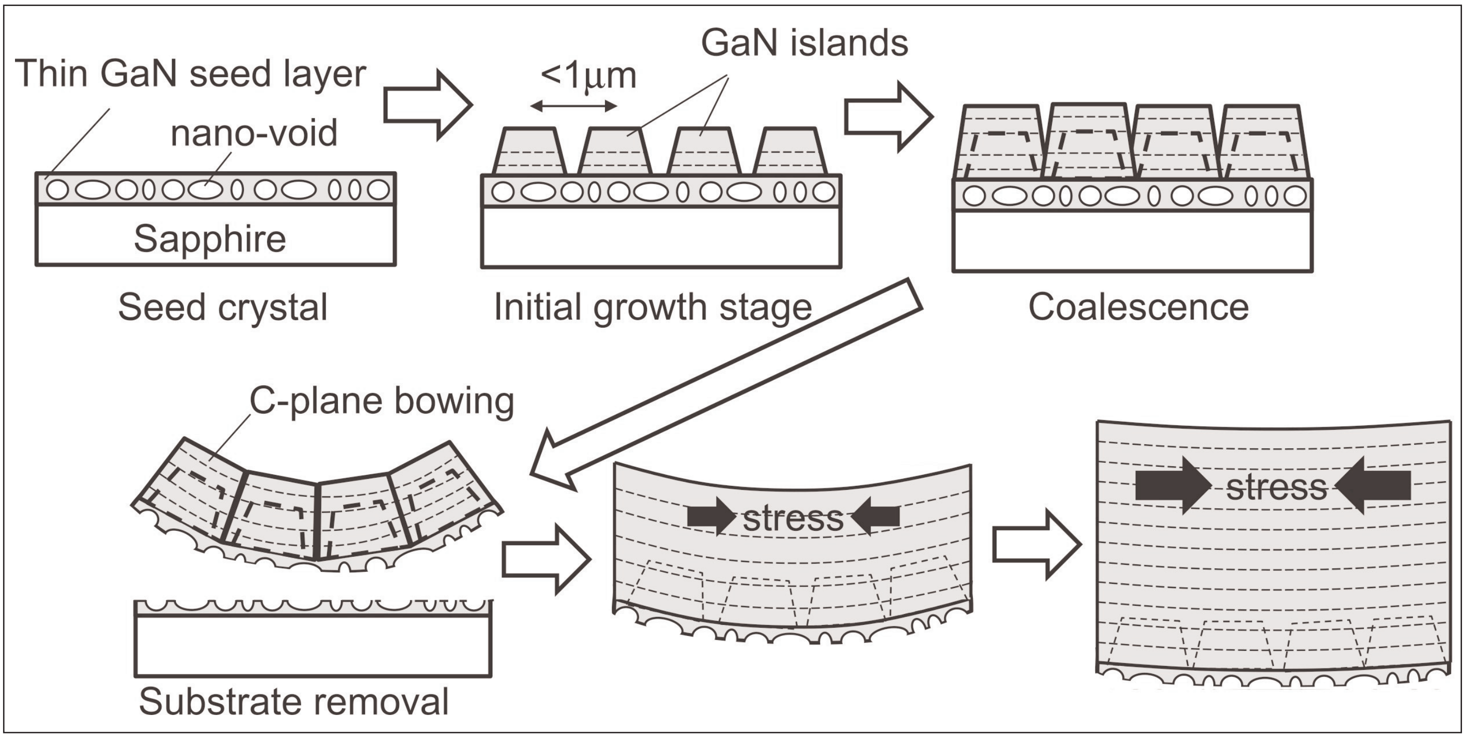

Figure 4. Sequence of void-assisted separation method.

The resulting GaN substrates ranged in thickness from 100µm (0.1mm) to more than 6mm.

The researchers found that the presence of macro-defects allowed the growth of thick GaN substrates without stress-induced cracking or breakage. Macro-defects reduce internal stress since crystal imperfection gives additional freedom for crystal deformation. However, macro-defects make it difficult to produce practical devices with high yield.

The team has therefore studied ways to use increased hardness to overcome the tradeoff by increasing the critical stress allowed in the GaN crystal. The hardness increase was achieved by controlling the HVPE growth conditions to reduce potential for plastic deformation. In previous work, the hardness of GaN substrates was increased from 19.7GPa to 20.1GPa and even 20.7GPa (samples A–C, respectively). The higher hardness value allowed the team to reduce threading dislocation densities even below $1x10^6/cm^2$, compared with $5x10^6/cm^2$ for the 19.7GPa initial sample. The 20.7GPa hardness process enabled GaN thicknesses up to 2mm without cracking.

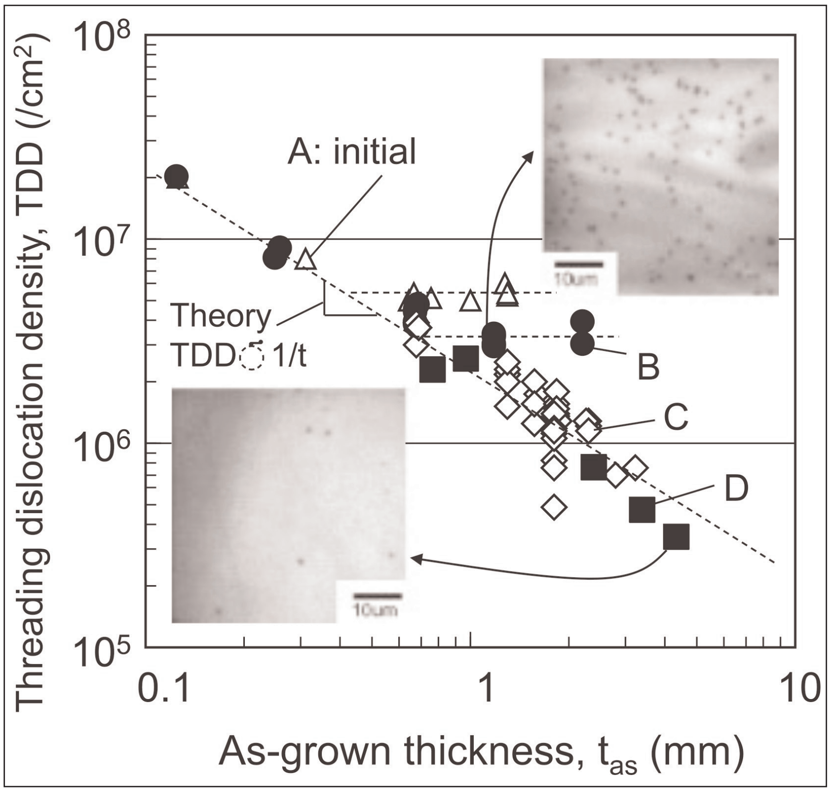

Figure 5. Relationships between as-grown thickness (t_{as}) and TDD for macro-defect-free GaN substrates grown by VAS method using conditions A–D. Insets: cathodoluminescence (CL) images for GaN substrates grown using conditions B and D.

Building on this work, the researchers achieved 22GPa hardness, allowing GaN thickness to reach 6mm without macro-defects in a 55mm-diameter substrate (2.17 inches). The sample (D) also showed much reduced TDD to the mid $10^5/cm^2$ range (Figure 5). Sample D did not show any tendency for the reduction of TDD with as-grown thickness to saturate. The new growth process for sample D also eliminated basal plane dislocations, allowing for increased thickness. The off-angle variation was less than 0.1º.

The researchers used their technology to realize 4-inch and 6-inch free-standing macro-defect-free GaN wafers with thicknesses of more than 3mm. Off-angle variation was 0.2º for the 4-inch substrate, and the TDD was in the $10^5/cm^2$ range. ■

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