Practical gallium nitride vertical field-effect transistors

Dr Quanzhong Jiang of Gate Source Drain Semiconductor Ltd discusses practical ways of exploiting the advantages of vertical field-effect transistors over existing lateral gallium nitride high-electron-mobility transistors.

The advent of gallium nitride (GaN) material and device technologies has led to novel lateral transistors. These include gallium nitride on silicon carbide (GaN-on-SiC) high-electron-mobility transistors (HEMTs) for high-power radio frequency (RF) amplifiers, and gallium nitride on silicon (GaN-on-Si) HEMTs for energy-efficient convertor/invertor circuits. However, due to the use of expensive, high-resistivity SiC substrates (~$2000 per 4" wafer), GaN-on-SiC RF transistors are very expensive (~$100–200 per 50W chip). GaN-on-Si HEMTs could break down at a few hundred volts or after a limited period of operation, and the breakdown mechanisms may be related to their high density of defects, the off-state electric field, and the use of thermally insulating AlGaN in the buffer for stress control and mitigation of buffer leakage.

Therefore, it is inevitable that vertical transistor designs have been proposed, such as the current-aperture vertical electron transistor (CAVET) [1] and trenched metal-oxide-semiconductor field-effect transistor (MOSFET) [2] etc. Like silicon or silicon carbide (SiC) vertical transistors, these require p-type materials acting as a current-blocking layer. However, it is problematic to incorporate p-type Mg:GaN into GaN vertical transistors due to magnesium diffusion and contamination during metal-organic vapour phase epitaxy (MOVPE) growth. This may lead to reduced electron mobility for two-dimensional electron gas (2DEG) channels or GaN drift layers. Alternative methods such as molecular beam epitaxy (MBE) incur high costs.

The recently published patent application (ref. PCT/GB2017/050316) describes the practical ways forward to form GaN vertical field-effect transistors (VFETs), and Figure 1 shows VFETs on Si(211) substrates for RF amplifiers and switching applications, respectively. The VFETs employ epitaxial lateral overgrown (ELOG) GaN to form an AlGaN/GaN two-dimensional free electron gas channel and a drift region in the drain for high-voltage applications. The use of ELOG GaN ensures a small on-resistance due to the large electron mobility for the 2DEG channel and the drift layer. Furthermore, the 2DEG channels are arranged in parallel with vertical GaN strips to facilitate easy heat dissipation into thermally conductive ELOG GaN [3],

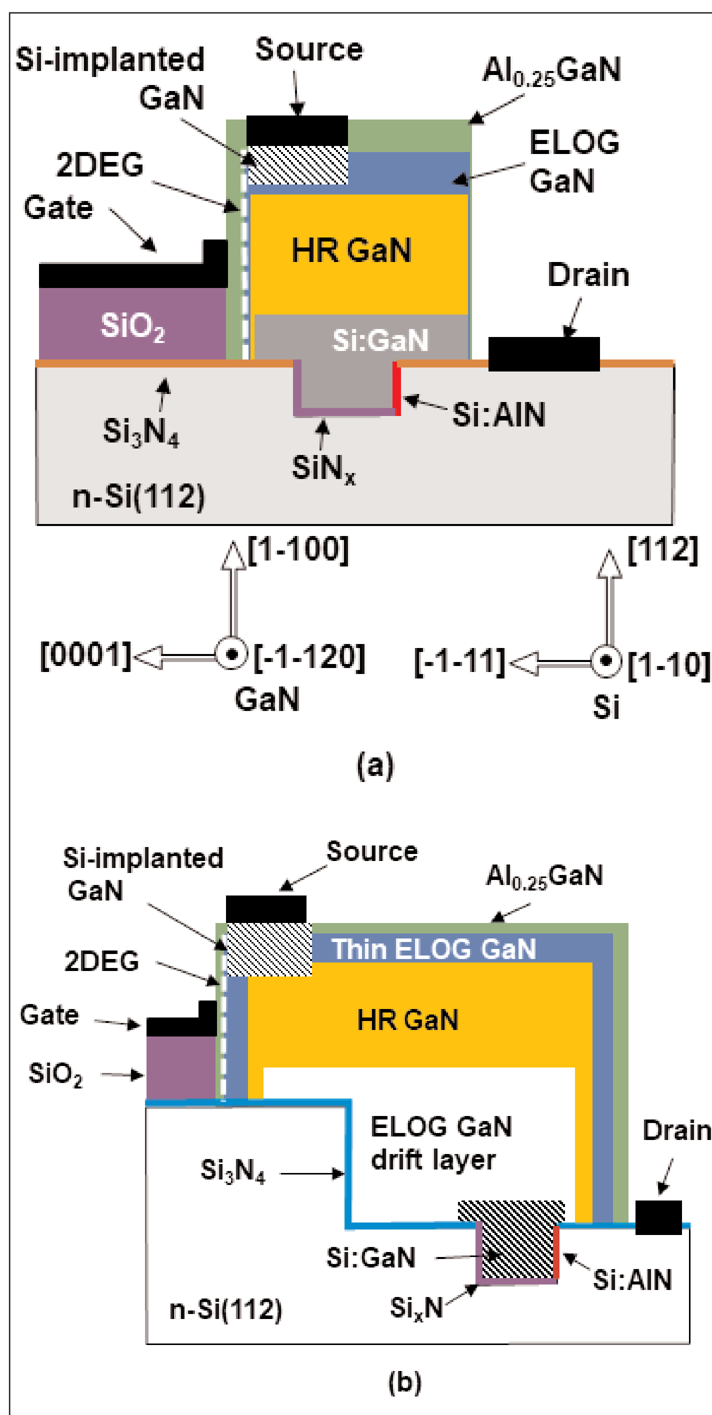

Figure 1 Sketches show VFETs formed on Si(211): (a) RF VFET with crystallographic relationship between Si(211) and GaN(1$\bar{1}$00); (b) VFET switching applications.

and subsequently the heat may be taken away through packaging material or the silicon substrate.

The formation procedure for the VFETs (Figure 1) begins with standard silicon processing (Bosch process and light KOH treatment). Provided that a Si ion implantation can be used to form the source, two separate MOVPE runs are sufficient for the structures shown in Figure 1: one is short to form a thin aluminium nitride (AlN) nucleation layer on Si($\bar{1}\bar{1}1$) facets and the other is to grow the whole structure by varying growth conditions to control lateral and vertical growth rates [4]. The source and drain electrodes can be easily formed without any difficulties. A narrow gate electrode may be fabricated by utilizing the huge difference between the deposition rates on the surfaces that face an electron-beam source crucible and on the other surface that is normal to an e-beam source crucible. For example, the formation of a gate could comprise: (i) depositing a base (SiO_2) (Figure 1) for the gate with a device template facing an e-beam source crucible — the thin SiO_2 layer deposited on the (0001) face may be briefly dissolved in HF solutions; (ii) depositing gate metals with the device template facing an e-beam source crucible at an angle of 45º; (iii) repeating step (i) to deposit a second layer of SiO_2 onto the gate metal layers to define the gate length; and (iv) dissolving exposed gate metals and removing the second layer of SiO_2 to complete the gate. So, a narrow gate may be formed without resorting to e-beam lithography and precise mask alignments.

The structures shown in Figure 1 may be optimized in different ways. For example, the silicon surface may be passivated with p-type dopants to reduce the current leakage from the GaN drift layer to n-type silicon substrates; also, Mg-doped GaN may be inserted into a highly resistive (HR) GaN layer without damaging the 2DEG channel, since the lateral growth of Mg-doped GaN will be minimized by adjusting MOVPE growth conditions [4]. ■

References

1 Chowdhury et al., IEEE Electron Device Letters 33(2012)41–43

2 Chowdhury et al., Trenched Vertical Power Field-Effect Transistors With Improved On-Resistance and Breakdown Voltage, US patent pub. No. US2017125574 (A1).

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