Developing complementary p-channel transistors for GaN-on-silicon power

Researchers use commercial epitaxial material designed for 650V normally-off p-type gallium nitride gate power devices.

Hong Kong University of Science and Technology (HKUST) report on p-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) produced on gallium nitride (GaN) on silicon (Si) substrates [Zheyang Zheng et al, IEEE Electron Device Letters, vol.41, p26, 2020]. The researchers used commercial 8-inch-diameter GaN-on-Si wafers with epitaxial structures designed for 650V normally-off p-GaN gate power high-electron-mobility transistors (HEMTs) (Figure 1).

GaN is being developed for high voltage and power handling based on the material's high critical electric field before breakdown. Devices with n-type channels with negatively charged carriers (electrons) have been intensively developed in recent years. Much progress has been made in developing devices with normally-off 'enhancement-mode' (E-mode) characteristics, rather than the more easily achieved normally-on 'depletion-mode' (D-mode). The E-mode is desired for lower power consumption and for fail-safe features.

The n-channel devices largely depend on the creation of 'two-dimensional electron gas' (2DEG) channels, which arise near the interface between GaN and a barrier layer, often aluminium gallium nitride (AlGaN). The 2DEG occurs due to band-bending effects arising from contrasts in the charge distribution in the chemical bonds holding the Ga, Al and N atoms together.

Devices with p-channels would enable complementary integrated circuit (IC) designs, which would further reduce power loss in logic control systems. Although some progress has recently been made in developing an analogous 2D hole gas for p-channels, effective devices remain to be achieved. The HKUST work focuses instead on using p-GaN material achieved using magnesium doping.

The team comments: "The p-GaN/AlGaN/GaN-on-Si platform paves the way to monolithically integrating E-mode pFET and nFET for possible GaN complementary and more robust GaN power ICs."

The GaN-on-Si material included a ~12nm AlGaN

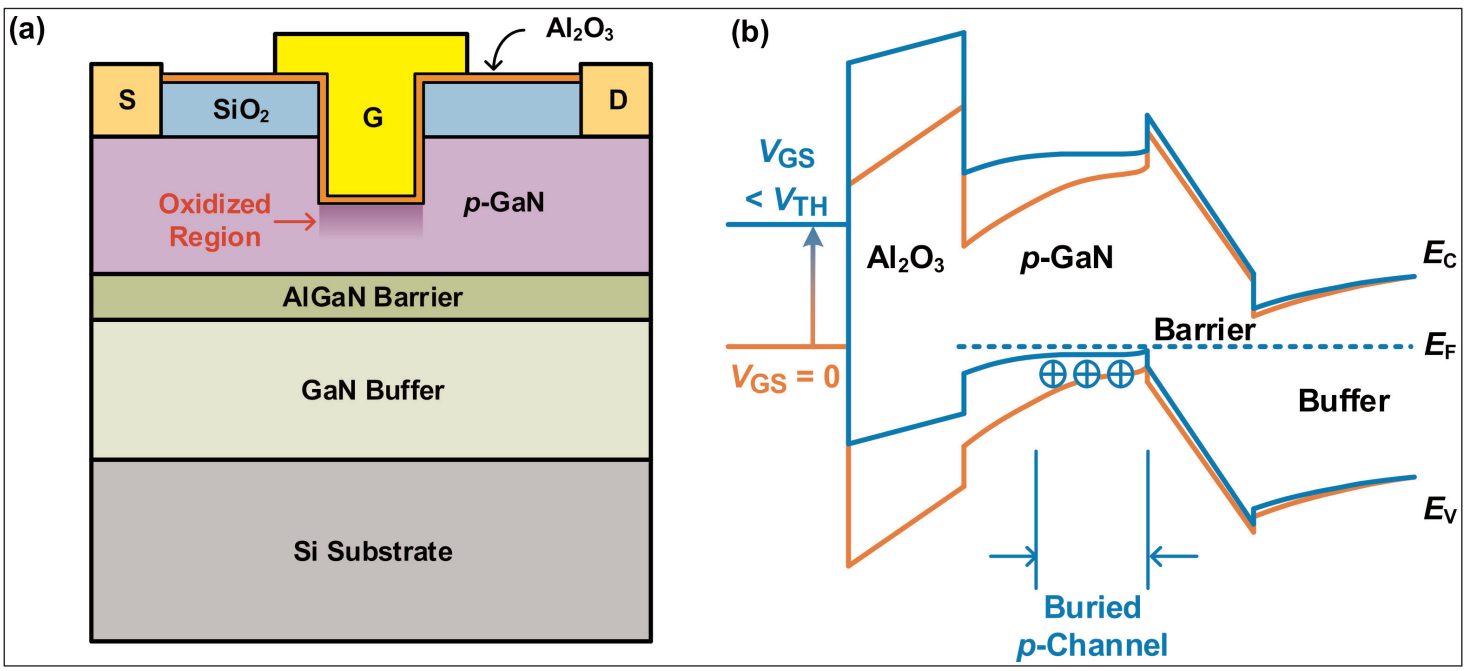

Figure 1. Schematic of (a) E-mode GaN pFET ($L_{GS}/L_G/L_{GD}$ = 4/2/4μm) and (b) energy band diagram at gated region of buried p-channel with 0V (OFF) and beyond threshold (ON) gate potentials (V_{GS}).

barrier and a ~85nm p-GaN top layer. The undoped GaN buffer was ~4.5μm thick. The structure was found to have a hole sheet density of $1.23x10^{13}/cm^2$ and mobility $10.2cm^2/V\text{-}s$, according to Hall measurements.

Standard p-GaN gate E-mode n-channel HEMTs realized on the substrate typically have threshold voltages of +1.7V and an on-current of 350mA/mm with 5V drain bias. The on/off current ratio is usually of order 10^9.

The HKUST p-channel devices were fabricated with 500°C-annealed nickel/gold ohmic source-drain (S–D) contacts evaporated onto the p-GaN, which had previously been subjected to a 5-minute buffered oxide etch, presumably to improve the surface and remove contaminants.

The gate (G) recess was defined by a 200nm plasma-enhanced chemical vapor deposition (PECVD) silicon dioxide (SiO_2) hard mask, which also served as surface passivation. The p-GaN recess was formed using inductively coupled plasma reactive-ion etch.

An oxygen plasma treatment increased the surface roughness at the bottom of the recess from 0.36nm root-mean-square to 0.41nm, according to atomic force microscopy. The recess depth was found to be about 54nm, leaving ~31nm of p-GaN material above the AlGaN barrier for the channel.

The gate structure was completed with 20nm atomic layer deposition (ALD) aluminium oxide (Al_2O_3) insulation and 400°C-annealed nickel/gold metal electrode. The electrical isolation of the devices was from fluorine ion implantation rather than mesa etching. The researchers used fluorine implant to avoid current leakage along rough mesa sidewalls. The implant occurred between the Al_2O_3 and gate metal deposition steps.

The device demonstrated a threshold voltage of –1.7V, giving normally-off enhancement-mode behavior at 0V gate. The oxygen plasma treatment enabled the negative threshold – without the treatment, the device became depletion-mode (normally-on at 0V gate) with the threshold at +2.2V. The on-current of the enhancement-mode device was 67% that of the depletion-mode transistor without oxygen plasma treatment.

The on-resistance for the E-mode device was a "relatively large" 2.4kΩ-mm at low drain bias. This reduced somewhat at –5V drain to 1.6kΩ-mm. The maximum drain current was 6.1mA/mm at –10V drain.

Affinity	Platform	V_{TH} [a] (V)	lg(I_{ON}/I_{OFF}) [b]	I_{ON} [c] (mA/mm)	*SS* (mV/dec)
Notre Dame [10]	*p*-/*i*-GaN /AlN Al_2O_3 MOS gate	0.89 (–80 V)	3 (–80 V)	3.87 (–80 V)	1415
RWTH [9]	*p*-/*i*-GaN/AlInGaN/ GaN/AlN, Schottky gate	–1.12 (–8V)	7 (–8V)	6.79 (–8V)	91.3
AIST [5]	*p*-/*i*-GaN/AlGaN/GaN Al_2O_3 MOS gate	> 4	N.A.	4.00	N.A.
RWTH [11]	*p*-/*i*-GaN/AlInGaN/ GaN/AlN, Schottky gate	–0.5	8	1.81	77
HRL [6]	*p*-/*i*-GaN/AlGaN/GaN AlN/SiN_x MIS gate	–0.36 (–0.1V)	6 (–0.1V)	1.65	304
AIST [7]	*p*-/*i*-GaN/AlGaN/GaN SiO_2 MOS gate	–0.75	3	0.09	817
Cornell [12]	*p*-/*i*-GaN/AlN SiO_2 MOS gate	1.32	4	9.10	1027
MIT [13]	*p*-GaN/AlGaN/GaN Al_2O_3 MOS gate	2.60 (–0.5V)	5 (–0.5V)	1.40	399
This work	*p*-GaN/AlGaN/GaN Al_2O_3 MOS gate	**–1.7**	**7**	**3.38**	**230**

[a] extracted at $|I_D| = 10$ μA/mm and $V_{DS} = -5$ V unless otherwise specified.
[b] (orders of magnitude) with $V_{DS} = -5$ V unless otherwise specified.
[c] at $V_{DS} = -5$ V and with overdriven V_{GS}, unless otherwise specified.

Table 1. Benchmark of p-channel GaN FETs.

The off-current with 0V gate was $1.2x10^{-7}$mA/mm. The team sees this low off-current as "delivering an ultra-low static power consumption required in CMOS logic gates."

The researchers explain the action of the oxygen plasma treatment: "It is known that oxygen induced into p-GaN could either behave as shallow donors to compensate the Mg acceptors or form inert Mg-O complexes to de-activate the Mg acceptors, both of which would result in depletion of holes. Hence, it is plausible to assume that the top oxidized GaN has its Mg doping compensated and the energy band bent downward to form a hole barrier that buries the p-GaN channel away from the top GaN surface."

The downward band bending pushes the depletion region under the recessed gate to extend through the p-GaN layer, reaching the AlGaN barrier. This enables enhancement-mode operation by turning off the buried p-channel at 0V gate potential.

The researchers compared their device with others previously presented in the scientific literature (Table 1). The team comments: "Among all the p-channel GaN MOSFETs, the one from this work exhibits the combination of high I_{ON}, high I_{ON}/I_{OFF}, the lowest sub-threshold swing (SS) and E-mode operation. Devices implemented on the platform with quaternary back-barrier and Schottky gate exhibit outstanding SS and I_{ON}, but suffers large gate leakage at the ON state." ■

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