Two-dimensional electronics for neuromorphic and other networking

Mike Cooke reports on work presented at December's IEEE International Electron Devices Meeting in San Francisco.

Atomic-scale layers are appearing in many levels of research towards the ubiquitous electronic social universe. Apart from creating smaller devices, the effort is also directed to the vaguely defined 'Internet of Things', where every electronic object has an IP address and even to the link-in of biological/neurological systems.

Many materials have a structure with strong bonds in a plane, but weaker bonds connecting the planes. Such structures offer the possibility of considering properties as being in two dimensions (2D). Examples include graphene (from graphite carbon), black phosphorus, and the transition-metal dichalcogenides based on molybdenum/tungsten atoms combined with two sulfur/selenium/tellurium atoms.

Here, we look at some of the contributions to this work reported at December's IEEE International Electron Devices Meeting (IEDM 2017) in San Francisco.

Electronic synapses

A number of groups put developing electronic synapse-like behavior among the aims of their work. These use hysteresis effects in the performance of the 2D structures to achieve different resistance states. 'Hysteresis' describes systems that 'remember' previous states — such as in the magnetization of ferromagnets. Although hysteresis is not wanted in many electronic applications, electronic memory does need some form of hysteresis. One option that has been widely studied over the years is resistive memory — variously described as 'memristors', resistive random access memory (RRAM), etc.

Northwestern University in the USA presented gate-tunable memristors based on monolayer molybdenum disulfide (MoS_2) [session 5.1]. Chemical vapor deposition (CVD) resulted in polycrystalline MoS_2 films with grain sizes of 3–5μm. The team fabricated memristors in a field-effect geometry with a MoS_2 channel (see Figure 1). Switching ratios for the devices reached up to ~500.

The CVD process was carried out on a silicon dioxide (SiO_2) layer on 300nm-thick silicon. The MoS_2 film was etched and titanium/gold (Ti/Au) source–drain electrodes deposited. Devices where the silicon substrate was used as a back-gate had channels that

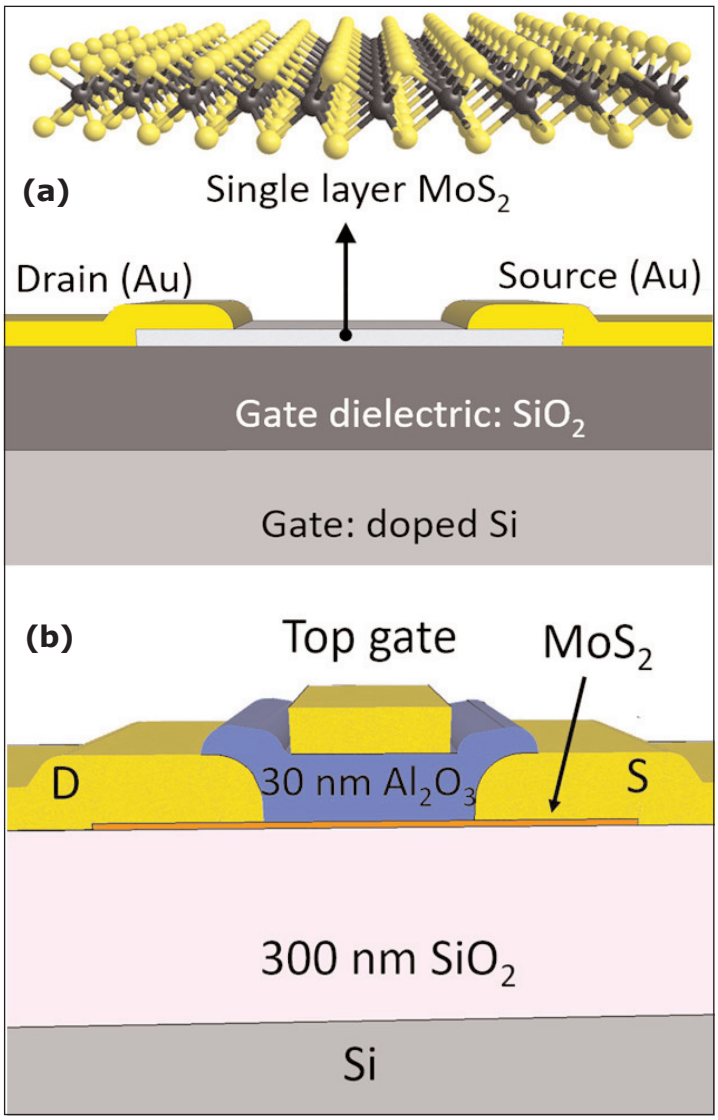

Figure 1. (a) Symbol and schematic of gate-tunable memristor on CVD-grown polycrystalline monolayer MoS_2 on a thermal oxide-coated doped Si substrate that acts as global bottom gate. (b) Top-gated MoS_2 memristor with 30nm-thick top gate Al O_x dielectric grown by ALD.

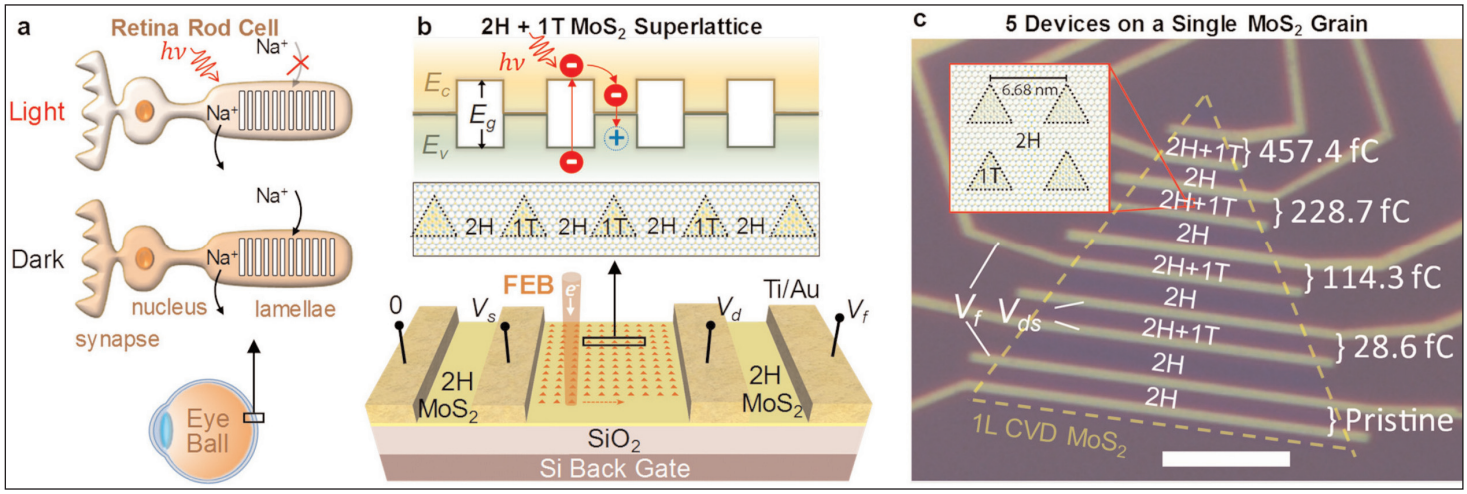

Figure 2. (a) Working principle of retina rod cell that accumulates charges with light stimulation and reduces charges in dark. (b) Schematics of device structure (bottom), 1T regions grown in triangle shape (middle), and band diagram of 2H/1T superlattice (top). (c) Optical image of five back-gated FETs. Scale bar 10μm.

were 5–15μm long and 50–100μm wide. Top-gated memristors were also fabricated with atomic layer deposition (ALD) of 30nm aluminium oxide (AlO_x) and deposition of gate metal.

The high-resistive and low-resistive states were controlled by the gate voltage over a range of three orders of magnitude for bottom-gated MoS_2 memristors and four orders for top-gated MoS_2 memristors. When the drain was positively biased, the source was a reverse-biased Schottky contact. Switching of the resistance occurs due to variation of the Schottky barrier height, which the researchers attribute tentatively to "vacancy migration and/or charge trapping".

The top-gated devices were able to tune the threshold voltage reversibly. The researchers admit that their devices are not ideal for high-performance RRAM. However, they comment: "The key innovation is in the continuous tunability of the resistive switching by the gate electrode that mimics realistic neural functions."

University of California Santa Barbara (UCSB) and Rice University in the USA claimed the first room-temperature light-sensitive memristive transistor, using quantum dot superlattice structures on monolayer MoS_2 [session 5.3]. The dots are used as charge traps that create memristive effects controllable by gate-induced electric fields and light stimulation.

The researchers see potential for artificial retina devices with artificial intelligence, and memristive receivers for optical-electrical neuromorphic interfaces (Figure 2). The short-term plasticity of the devices is seen as mimicking the properties of synaptic connections in neurological systems. Previous quantum dot memristive transistors have been produced before, but the operation was cryogenic.

The MoS_2 was produced by CVD on 285nm SiO_2 on Si. The quantum dots were produced by converting the semiconducting 2H (trigonal prismatic D_{3h}) phase of the deposited MoS_2 into metallic 1T (octahedral O_h) phase using a focused electron beam. A silicon substrate back-gate was used. The contact electrodes were Ti/Au.

Another approach to electronic synapses, using 2D hexagonal boron nitride (h-BN) was presented by Soochow University in China, Stanford University in the USA, Singapore University and Università di Modena e Reggio Emilia in Italy [session 5.4]. This was the first use of h-BN for synaptic resistive switching, according to the researchers. Stacks of h-BN layers were grown by CVD on copper. In the fabricated devices the copper served as the bottom electrode, while the top electrode was Ti/Au.

Unlike devices based on transition-metal oxides, the h-BN electronic synapse demonstrated both volatile and non-volatile resistive switching. Simple short-term and long-term plasticity rules can be applied through different electrical stresses varying the current-voltage magnitudes and limits along with pulse durations and periods. Conductive filaments form through boron vacancies in stacks of h-BN layers, altering the resistance. Differences in performance with the polarity of the signals was attributed to the different diffusion properties of the electrode metals into the h-BN stack.

Stanford University in the USA also says it has demonstrated "the first 1-transistor-1-resistor (1T1R) memory cell using the monolayer MoS_2 field-effect transistor (FET) and resistive random access memory (RRAM)" [session 19.5].

The team believes that the development could lead to "tight integration of memory with logic in a monolithic 3D integrated chip". The RRAMs were based on oxygen vacancy formation in ALD hafnium dioxide (HfO_2). The addition of transistors is designed to suppress sneak path leakage currents.

The monolayer MoS_2 was grown by CVD on a 300nm SiO_2/Si substrate. The fabrication process temperature did not exceed 200ºC.

The RRAM component had median set and reset voltages of 1.18V and −0.9V, respectively. The median high over low resistance ratio was 148. The retention time was ~10^4s at 125ºC. The transistor had an on/off current ratio of ~10^6 with the top gate biased at +2V and −2V. The drive current reached 190μA/μm with 2.5V drain bias.

In the 1T1R configuration, the high over low resistance ratio was more than 10^4. The configuration also enabled multi-level resistance states that could be used for electronic synapses and neuromorphic computing or for in-memory computing — storage of data in fast RAM rather than in complex databases on relatively slow disk drives.

On the basis of simulations, the researchers believe that, with suitable device scaling, multi-layer 3D-integration structures could be achieved.

Photodetectors

Infrared

National University of Singapore presented a black phosphorus carbide (b-PC) phototransistor designed for infrared spectroscopy [session 8.4]. The researchers believe that the b-PC could detect wavelengths over the range 2000–8000nm, allowing molecular vibration fingerprinting. Only a few 2D materials have the narrow bandgap needed to cover this range – others being graphene and black arsenic phosphorus. The b-PC material was achieved using a carbon doping technique.

The team reports that the b-PC phototransistor

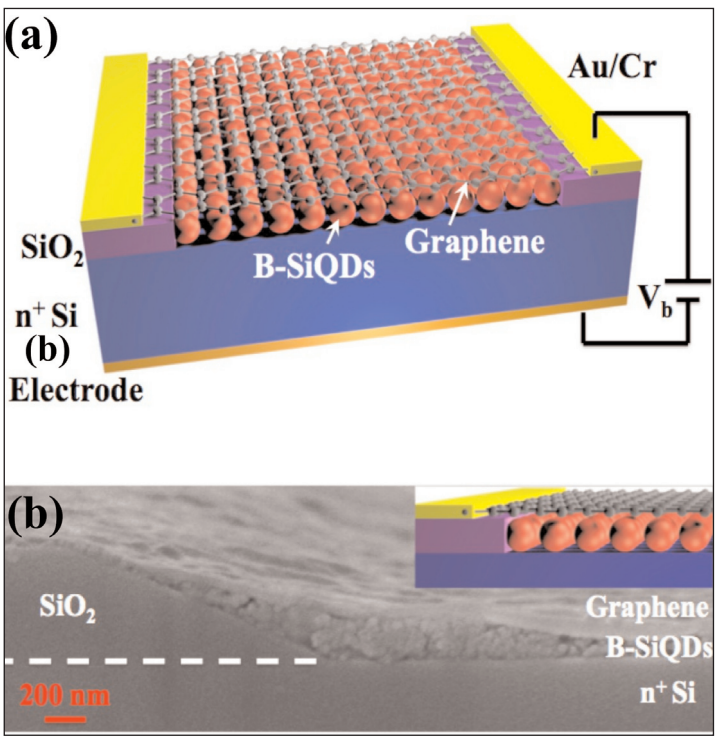

Figure 3. Schematic of Gr/B-SiQDs/Si device structure, and (b) corresponding cross-sectional scanning electron microscope image.

achieved a responsivity of 2163A/W and a short response time of 5.6ps. The device was operated at room temperature.

The researchers comment: "Under the same excitation power, its responsivity and detectivity performance in ambient and room-temperature conditions are currently ahead of all recent top-performing photodetectors based on 2D materials, showing promise for future Internet-of-Things (IoT) applications."

Zhejiang University in China has used graphene (Gr) on boron-doped silicon quantum dots (B-SiQDs, Figure 3) to give a Schottky-PN cascade heterojunction that can detect short-wavelength infrared (SWIR) [session 8.7]. The operating range was 800–1870nm with a response up to 0.6A/W at 900nm wavelength. The researchers see potential for spectroscopy, environmental monitoring, industrial inspection, medical diagnostics and bio-imaging.

The 6nm spherical p-type dots were formed from boron hyper-doping through a non-thermal plasma method. The silicon substrate was n-type. The researchers comment: "The built-in potential of Schottky junction, induced by the graphene (Gr) and n-type Si wafer, extracts the photo-electrons into Gr, leaving holes trapped in B-SiQDs. Then electron injections increase the Fermi energy of Gr, thus lowering the Schottky barrier height and leading to an exponential amplification of SWIR photocurrent."

Solar-blind UV

King Abdullah University of Science and Technology (KAUST) in Saudi Arabia and University of Maryland in the USA reported on flexible solar-blind deep-ultraviolet sensors fabricated from boron nitride nanopaper [session 8.5] The BN sheets combined with 1D nanofibrillated cellulose into a nanopaper structure had a thermal conductivity of 146W/mK, compared with 0.03W/mK for conventional paper and ~0.2W/mK for plastic. The cellulose fibers were also thought to enhance the strength of the structure by linking the nanosheets together.

The device used 300nm-thick platinum electrodes. Dark current was of the order of pico-Amps, compared with micro-Amps for devices constructed from BN nanosheets. The devices were stable up to 200ºC, and performance degradation compared with 25ºC was superior to photodetectors based on β-phase gallium oxide, silicon carbide, gallium nitride or silicon.

The researchers suggest applications of the device include military sensing, automation, short-range communications, security, and environmental detection.

A graphene/ultra-thin silicon metal–semiconductor–metal ultraviolet (UV) photodetector was described by a team from China's Zhejiang University, Chinese Academy of Sciences, Tsinghua University, and State University of New York (SUNY) in the USA [session 8.6]. The UV/visible rejection ratio was about 100, compara-

ble to the state-of-the-art Schottky photodetectors. The team also replaced a CCD array from a digital camera with the graphene/Si sensor to create an imaging platform.

CVD graphene was used as a thin active electrode that forms a Schottky junction with the underlying ultra-thin silicon. The silicon bar structures were patterned on p-type silicon-on-insulator substrates that were subsequently transferred to polyimide material. The CVD graphene sheet was then transferred onto the silicon bars and etched into interdigitated patterns. Chromium (Cr) and gold (Au) were evaporated as contacts.

The device uses the short penetration depth of UV in silicon and the ultra-shallow junction provided by the graphene to separate electron-hole pairs without significant recombination to give high response. Some hot carriers are also produced in the graphene with up to 10% photon absorption. The maximum response was 0.47A/W with 3V bias and 365nm-wavelength illumination. The short UV penetration depth and the 20nm ultra-thinness of the silicon bars made the devices relatively visible-blind.

Subthermionic subthreshold swing

University of Minnesota in the USA presented black phosphorus tunneling FETs (TFETs) that demonstrated subtheshold swings (SSs) near the thermionic limit of 22mV/decade at 110K [session 15.7]. Subthreshold swing represents the sharpness of the transition from off current to on current below the threshold gate potential — with low values usually being desired for a steep turn-on. It is possible for TFETs to have subthermionic SS, since the limit really only applies to non-tunneling devices. At room temperature (~300K) the limit increases proportionately to around 60mV/decade.

The TFETs used transport directions for the 9nm channels that were aligned to the armchair and zigzag crystal orientation. The performance was anisotropic with the maximum 0.9μA/μm on-current being achieved with armchair orientation. The bandgap of black phosphorus varies from 0.3eV in bulk material, up to 2.0eV for monolayers.

Purdue University in the USA and National Nano Device Laboratories in Taiwan presented subthermionic (<60mV/decade) SS negative-capacitance FETs (NCFETs) based on a few-layer MoS_2 channel and ferroelectric hafnium zirconium oxide (HZO) underlayer [session 23.5]. The device also used an internal metal gate (Figure 4). The forward-gate sweep SS was 37.6mV/decade, while the reverse SS was 42.2mV/decade. In high-speed switching, the reverse SS was as low as 8.3mV/decade, although with larger hysteresis that reduced the transistor's performance.

The polycrystalline HZO was deposited by 250ºC ALD. Amorphous ALD AlO_x was used for capacitance matching. The MoS_2 channel was derived by mechanical exfoliation on scotch tape.

The hysteresis problem was attributed to parasitic capacitance. The researchers comment: "High parasitic capacitance prevents the NC-FETs to work at high speed so that the optimization of parasitic capacitance to balance between SS and working speed in NC-FETs is required."

China's Nanjing University, Fudan University and Hong Kong Polytechnic University also developed MoS_2 NCFETs with subthermionic performance [session 23.6]. The structure was essentially the same as for the Purdue University and National Nano Device Laboratories NCFET without the internal metal gate. The fabrication process was also similar with ALD 4nm AlO_x and 20nm HZO or, for lower SS, 2nm AlO_x and 20nm HZO. The channel length was 1.7μm or 2.6μm, respectively.

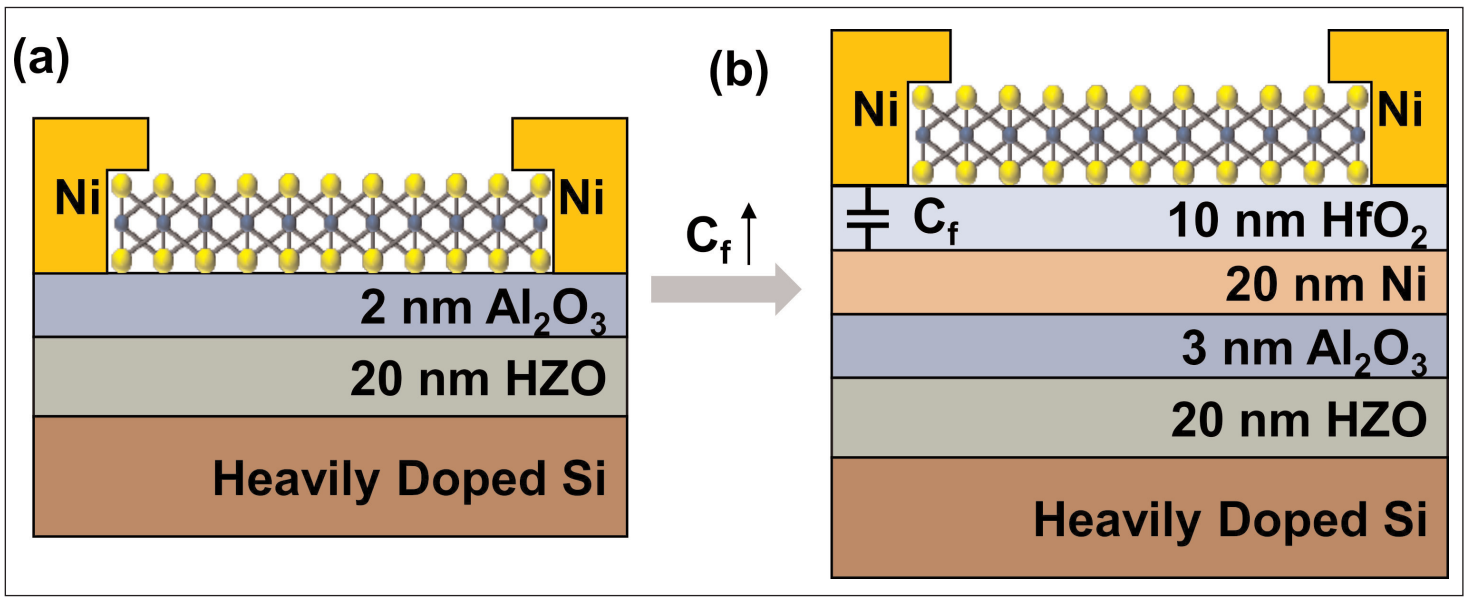

Figure 4. Schematic of MoS_2 NCFETs (a) without and (b) with internal metal gate.

The SS in the Nanjing et al case was as low as 23mV/decade and the drain current spanned a range of six orders of magnitude. The on/off current ratio was more than 10^9 with a maximum drain current of 250μA/μm (180μA/μm for 2nm AlO_x). The performance was "nearly hysteresis-free" (less than 24mV for 4nm AlO_x, 77mV for 2nm) up to 1V drain bias, the team reports.

The researchers see their devices as potential components for future ultra-low-power applications with sub-0.5V operation.

Combining carbon nanotubes and graphene

Peking University in China has scaled the gate lengths of carbon nanotube (CNT) transistors down to 5nm by using graphene contacts [session 5.5]. The researchers comment: "Scaling trend study reveals that sub-10nm CNT CMOS FETs significantly outperform Si CMOS FETs with the same gate length but at much lower supply voltage V_{ds} (0.4V versus 0.7V), with an excellent subthreshold slope swing (SS) of about 73mV/decade even with the gate length being scaled down to 5nm."

Single-walled tubes were grown on SiO_2/Si. Semiconducting tubes were identified by field-effect measurements where the silicon substrate was used as a back-gate. Graphene source/drain (S/D) contacts were created by transferring CVD-grown material and patterning with electron-beam lithography (Figure 5). The gate stack consisted of 4nm yttrium oxide (Y_2O_3) and palladium (Pd) electrode.

The graphene-contacted CNT FETs enabled SS values less than 80mV/decade even down to 5nm gate length, unlike metal-based contacts on CNT or even silicon FETs. The researchers comment: "This improvement is due largely to the much thinned S/D, i.e. graphene S/D, and the better gate control due to the use of Y_2O_3 as the gate dielectric."

The team further claims that the performance of the device in terms of intrinsic gate delay and energy-delay product are close to the theoretical limits based on Shannon–von Neumann–Landauer thermodynamic and Heisenberg quantum-uncertainty analyses. They report: "In particular, the gate delay of the 5nm CNT FET is scaled down to 43fs, which should be compared with the theoretical limit of 40fs... [O]n average, there exist only 1.35 electrons in the 5nm CNT channel in its on state, suggesting that typically a single electron is involved during the transition of the CNT FET."

Peking University also reported solution-processed CNT transistors with current density reaching 1.7mA/μm and peak transconductance (g_m) 0.8mS/μm with 120nm gate length (L_g) [session 5.6]. The researchers increased the CNT density to 160/μm, and adopted stacked contacts and double gates (SCDGs) to claim record performance (Figure 6). "In contrast to Si FETs with similar L_g, our SCDG CNT FETs exhibited not only higher I_{on} and but also higher g_m, which are achieved by CNT-based FETs for the first time," the team says.

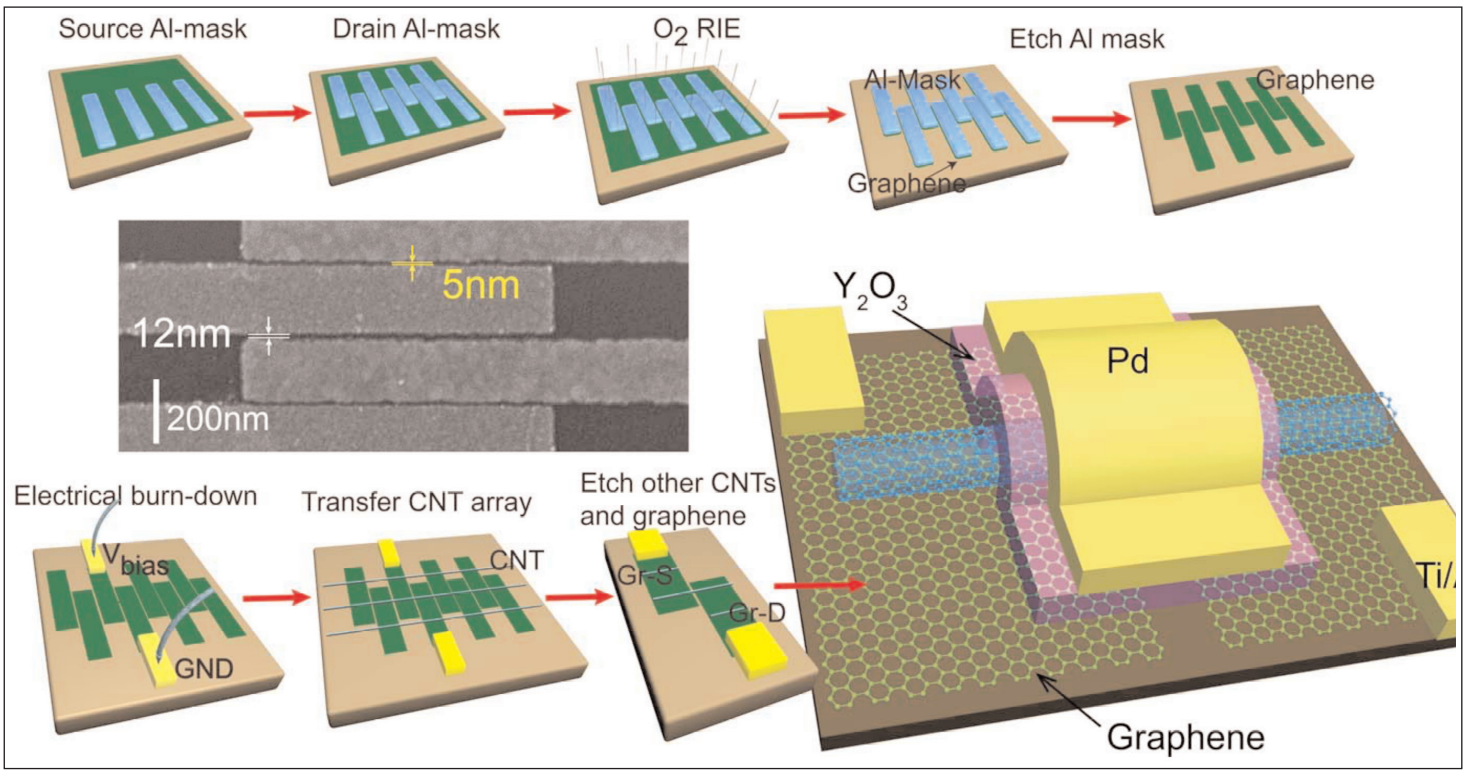

Figure 5. Process flow of GC CNT FET. (1) Transferring CVD graphene to SiO_2/Si substrate. (2) Forming source mask. (3) Forming drain mask. (4) Forming gaps on graphene. (5) Forming connecting wires and pads, and performing electrical burn-down process. (6) Transferring CNTs to graphene source and drain arrays. (7) Forming Y_2O_3 gate insulator. (8) Forming gate electrodes and finishing GC-CNT FETs.

The bottom gate and contacts were Ti/Au/Pd and the top contacts were Pd/Au while the top gate was Pd. The gate dielectrics were ALD HfO_2.

University of California Santa Barbara claimed the first all-carbon interconnect scheme integrating graphene wires and carbon nanotube vias [session 14.3]. The team found through simulation analysis that the hybrid interconnects surpassed the performance, energy efficiency and reliability of copper for 5nm-node VLSI technology.

Nickel was used to make the contact between the multi-layer graphene and carbon nanotubes. This metal has high carbon solubility when annealed at temperatures above 400ºC. Via-chain structures were constructed using 10nm-thick CVD multi-layer graphene (MLG) transferred onto thermal SiO_2. It is hoped in future to use low-temperature 435ºC synthesis of graphene directly on a dielectric substrate.

The MLG was patterned and etched. Further SiO_2 insulation was created using plasma-enhanced CVD. The 0.7μm-high 40nm-diameter vertical CNT vias were fabricated by etching holes and depositing 5nm nickel at the bottom as catalyst for CNT plasma-enhanced CVD. The CNT was capped with nickel for the contact to the upper-level MLG.

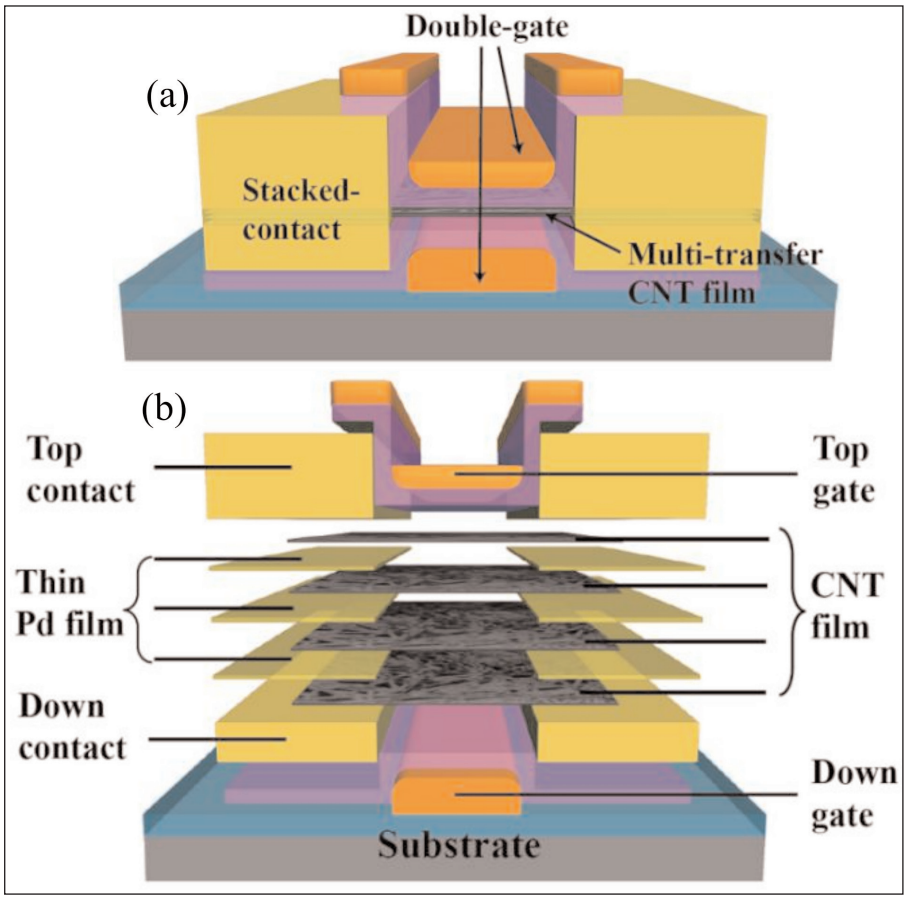

Figure 6. (a) Schematic of SCDG CNT FET, and (b) decomposed layer structures.

The nickel contacts were annealed by a series of steps passing current through the structure for 100 seconds to create self-heating above 400ºC. Before annealing, the via-chain resistance was 9.56kΩ — this reduced to 7.5kΩ after annealing. The experimental structures were 2μm wide.

Extremely scaled interconnects are expected to suffer from self-heating effects that impact performance. The researchers comment: "By using all-carbon interconnects, both current crowding and local self-heating effects are alleviated for both with and without via misalignment, because (1) barrier layers are eliminated thus creating larger contact area, and (2) MLG wires and CNT vias exhibit relatively high horizontal and vertical thermal conductivity, respectively."

Vanadium dioxide

École polytechnique fédérale de Lausanne (EPFL) in Switzerland combined MoS_2 with vanadium dioxide (VO_2) to create n–n van der Waals (vdW) heterojunction devices such as tunable rectifiers, photodiodes and FETs [session 36.1].

Tunable diode characteristics with rectification ratios of more than 10^3 were derived from a favorable band alignment and a sharp, clean atomic-level vdW interface (Figure 7). The VO_2 could also be forced to transition from an insulating to a metallic phase under high voltage or high temperature (>68ºC) stress, giving Schottky behavior. Photosensitivity was found in the 500–650nm wavelength range.

The team also reports "the first ever field-effect transistor based on gated MoS_2/VO_2 heterojunctions, which is a true low-power FET exploiting a phase-change material where the electrostatic doping effect of the gate on the junction results in a subthreshold slope (SS) of 130mV/dec at room temperature, $I_{ON}/I_{OFF} > 10^3$ and $I_{OFF} < 5pA/\mu m$ at $V_D=1.5V$."

The 75nm VO_2 was sputtered onto a 2μm wet oxide layer on a silicon substrate. The MoS_2 came from mechanical exfoliation. For three-terminal devices an AlO_x/HfO_2 gate stack was fabricated by sputtering and oxidizing a 2nm Al layer and ALD, respectively. The gate metal was 1nm tantalum and 140nm gold.

Paper substrate

University of Texas in the USA claims the first demonstration of record GigaHertz graphene and MoS_2 transistors on paper substrates [session 5.2]. The researchers used commercially available glossy paper as a substrate for a range of wet and thermal growth processes such as ALD. The substrate was first coated with polyimide to improve surface smoothness.

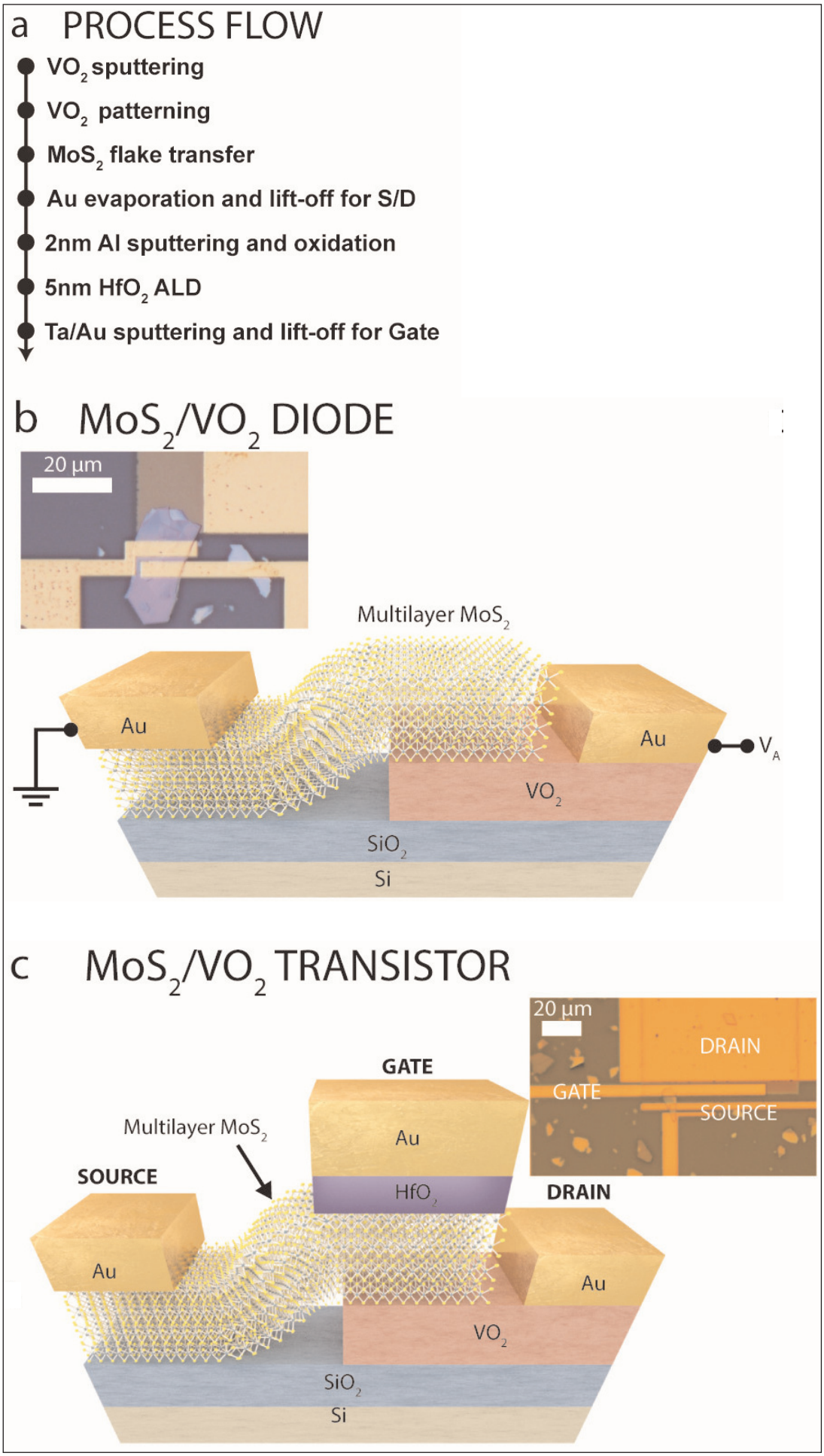

Figure 7. (a) Fabrication of MoS_2/VO_2 heterojunction devices. (b) 3D schematic view of two-terminal device and optical image (inset). (c) Three-terminal device schematic and optical image.

Graphene transistors were fabricated from CVD graphene grown on copper foil transferred onto an embedded gate stack consisting of Cr/Au metal and ALD AlO_x insulator. The source–drain electrodes were nickel/gold. The devices were estimated to have hole and electron mobilities of 3600cm^2/V-s and 2380cm^2/V-s, respectively. The channel length was 250nm and the width was 10µm. The current density achieved is claimed to be a record for paper-based 2D atomic materials. The intrinsic cut-off frequency was ~25GHz.

The MoS_2 devices were fabricated similarly to the graphene devices using material grown by CVD on SiO_2/Si. The extrinsic power gain cut-off of the device reached a record 7.2GHz.

The researchers hope flexible paper-substrate electronics could open up roll-to-roll processing with opportunities for high-performance nanoelectronics on low-cost paper substrates deployed in 'Internet of Things' and disposable sensor technology. ■

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