Atomic scaling of future electronic materials to lower dimensions

Mike Cooke reports on increasing interest in graphene, nanotubes and other planar and linear structures at the IEDM conference in San Francisco.

As microelectronics scales down to atomic scales, engineers and scientists must increasingly deal with phenomena that are better described in terms of two-, one- and even zero-dimensional models. The loop joining experiment, theory and models provide the language needed for coordinating and creating applications. There is much interest at the moment in potential electronic applications of two-dimensional (2D) materials that are formed from strong intra-plane bonds and weaker inter-plane adhesion. This was reflected at the recent IEEE International Electron Devices Meeting (IEDM 2016) in San Francisco last December.

Researchers have used '2D' structures in III-V compound semiconductors for some time, in the form of quantum wells with charge carriers confined to thin nanometer-scale layers. In complementary metal-oxide-semiconductor (CMOS) transistors the channel consists of a thin 'inversion layer' under the gate. However, new materials like graphene, along with transition-metal dichalcogenides (TMDs) and hexagonal boron nitride (BN), allow the confinement to be squeezed by a factor of ten to the atomic scale.

Since the development is relatively new, several presentations and almost all of session 14 concentrated on theory and modeling. However, we focus here on experimental achievements.

Graphene

The Indian Institute of Science claims record low resistance for chemical vapor deposition (CVD) graphene contacts with metal at room temperature [session 5.3]. The researchers used various techniques to massage the chemical bonds by engineering the carbon atomic orbitals from the sp^2- to sp-hybridized form. The sp^n hybridization description is commonly used in carbon (quantum) chemistry — sp^3 gives the diamond structure and sp^2 gives graphene/graphite. The sp-type bond is seen in the linear acetylene structure HC–CH with a triple bond between the carbons.

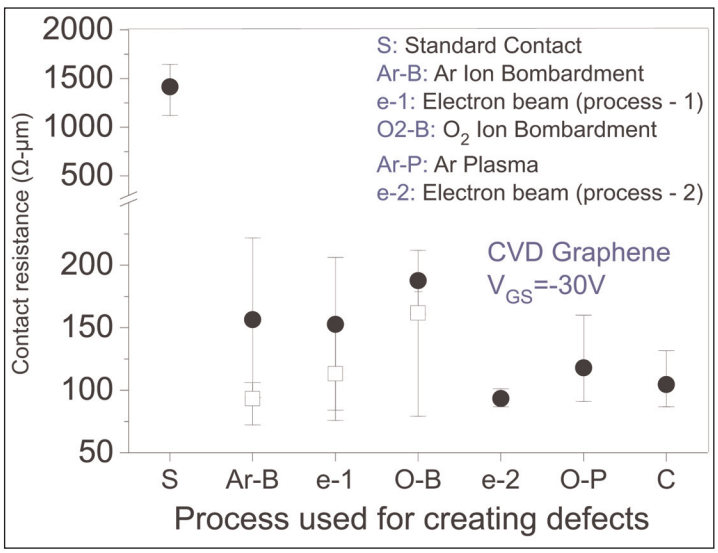

Figure 1. Metal–graphene contact resistance of standard versus engineered contacts from different processes.

The sp hybridized carbon orbitals form a more conducting bond with metal. Graphene edges contain sp hybridized carbon atoms. The experimental realization of sp hybridization was achieved by increasing the edges of the graphene.

Three techniques were tried to give graphene with increased sp hybridization: plasma/ion bombardment with oxygen or argon, electron-beam, and increasing the edge perimeter through lithography of comb patterns. The plasma/ion and electron-beam techniques increase sp hybridization through introducing defects in the graphene structure.

All the methods were found to reduce contact resistance — 78Ω-μm for oxygen plasma, 84Ω-μm for electron-beam treatments (see Figure 1). These achievements are claimed as record lows for metal–graphene contacts. The 84Ω-μm value is claimed as "138% and 28% better than best reported till date while using CVD and epitaxial graphene, respectively."

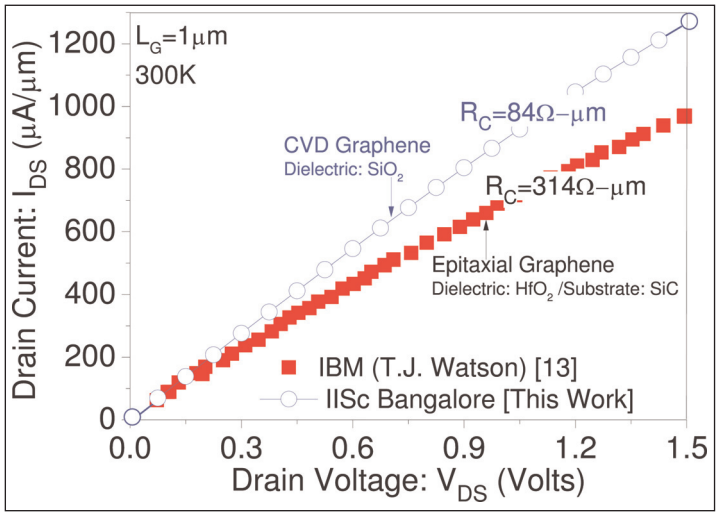

Figure 2. Transistor output characteristics of CVD graphene on SiO_2 FET with engineered contact compared with the best reported in literature for epitaxial graphene on SiC substrate.

The researchers also report that their contact engineering has led to CVD graphene transistors offering record high performance (Figure 2), "better than the best reported till date" for epitaxial graphene on silicon carbide.

Stanford University and Lam Research Corp have used graphene grown on copper (Cu) wiring to reduce electro-migration that can degrade performance of advanced integrated circuit interconnects [session 9.5]. The process was carried out below 400ºC to meet back-end-of-line (BEOL) thermal budgets in CMOS manufacturing.

The test structures consisted of sputtered tantalum (Ta) and Cu on silicon dioxide on silicon (SiO_2/Si) substrate (Figure 3). The 5nm tantalum was used as an adhesion layer. After patterning, the graphene was applied by CVD. Plasma-enhanced CVD silicon nitride (SiN_x) provided a capping layer.

The researchers report that the graphene/Cu composite exhibited 2x lower resistivity, 1.4x higher breakdown current density and 40x longer electro-migration (EM) lifetime than as-deposited Cu. The EM performance at 150ºC with 20MA/cm^2 stress was also 10x better than 2nm cobalt tungsten phosphide (CoWP) on copper.

An industry-standard 3nm CoWP layer had comparable EM characteristics to the graphene coating.

With SiN_x capping, a temperature of 200ºC and 36MA/cm^2 was used to shorten the time to EM failure. The SiN_x improved the performance of CoWP layers on Cu more than for the graphene, and the mean time to failure (MTTF) of graphene layers was 1.3x less than for 3nm CoWP.

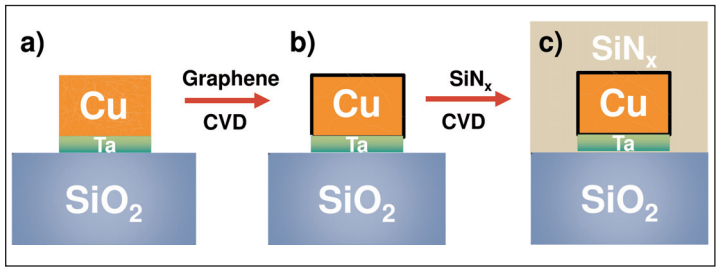

Figure 3. Cross-sectional view of process steps for fabricating test structure. (a) Ta/Cu is sputtered onto SiO_2/Si substrate followed by metal lift-off. (b) Graphene is grown directly on patterned Cu wires by CVD below 400ºC. (c) Structure is then capped with SiN_x as protection layer against oxidation under high-temperature stress testing.

The breakdown current density was 65MA/cm^2, compared with 52MA/cm^2 for wires capped with amorphous carbon or CoWP and 48MA/cm^2 for the Cu as-deposited.

Fujitsu Laboratories Ltd presented gas sensors based on graphene-gate transistors [session 18.2]. The absorption of molecules on the graphene alters the work function and hence the transistor threshold voltage.

The devices were based on 0.6μm silicon MOS field-effect transistors (FETs), but with 13.5nm graphene replacing the usual polysilicon gate electrode (Figure 4). The graphene came from CVD on Cu.

The device was particularly sensitive to ammonia (NH_3) and nitrogen dioxide (NO_2), but not sulfur dioxide, hydrogen sulfide or acetaldehyde (Figure 5). NO_2 is an air pollutant that arises from motor vehicle emissions and smoking, causing inflammation of airways and asthma.

The team reports: "We have actually found that this sensor can have a sensitivity more than one magnitude higher than that of resistivity-based graphene gas sensors and commercially available gas sensors."

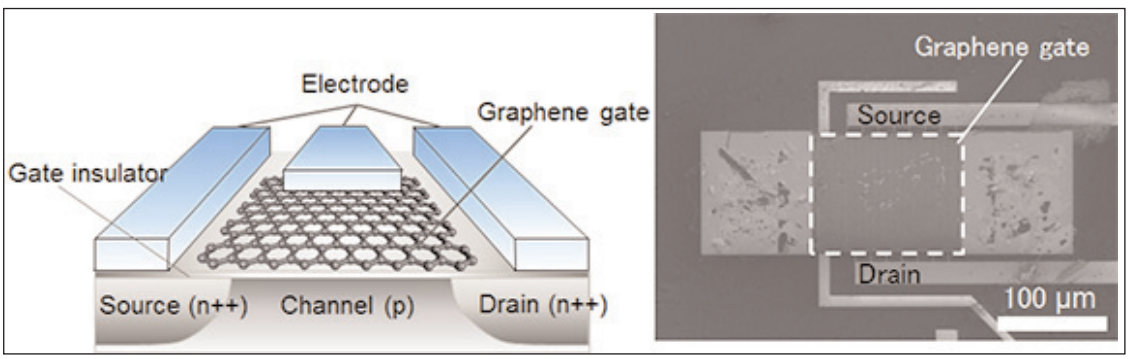

Figure 4. Schematic and scanning electron microscope (SEM) images of graphene-gate transistor sensor.

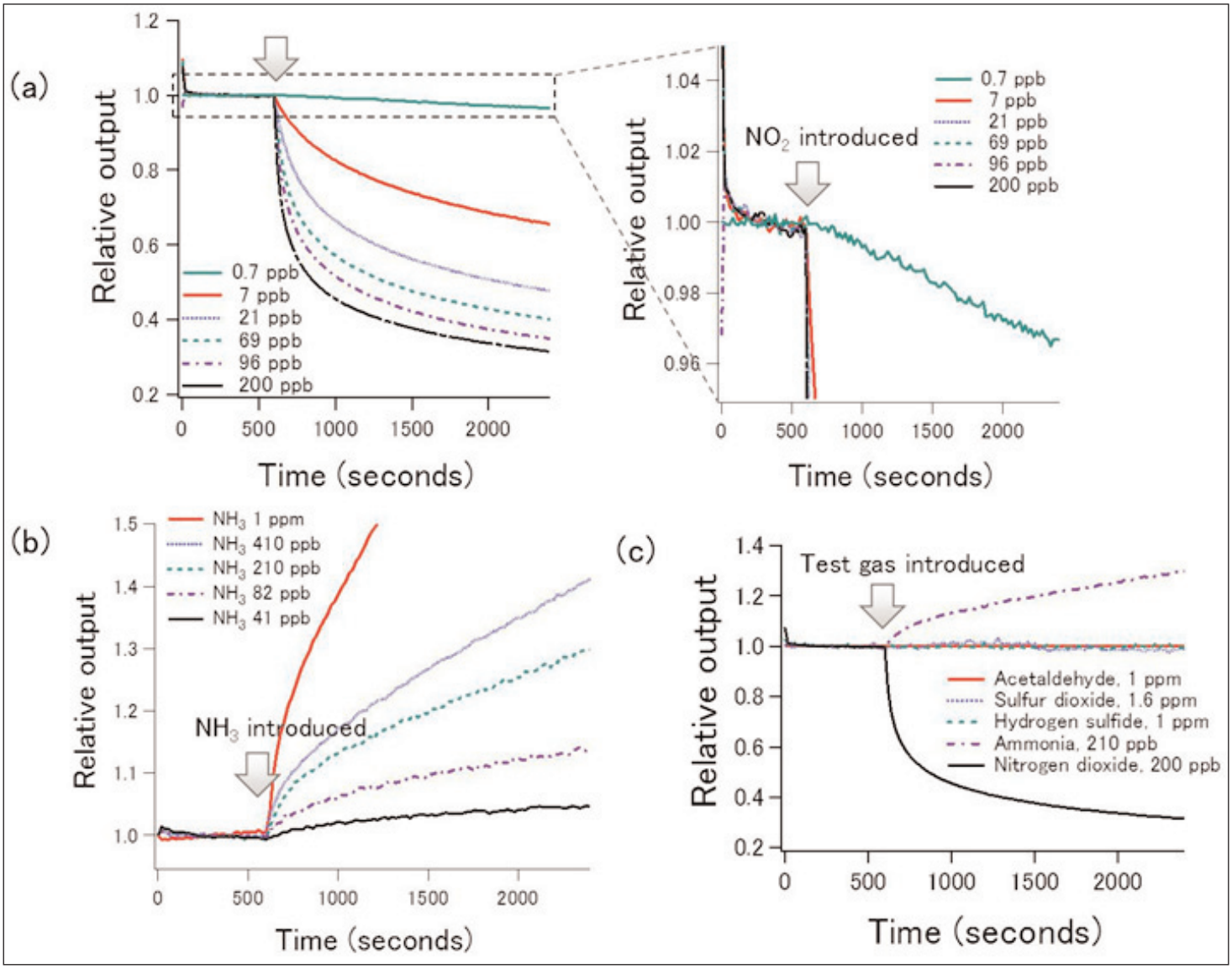

Figure 5. (a) Responsiveness of graphene-gate transistor sensor to NO_2 with magnification. (b) Response to NH_3. (c) Response to other gases.

A Fujitsu press release adds: "This technology's sensitivity to NO_2 is an order of magnitude greater than conventional resistivity-based graphene sensors, at less than 1ppb, and the commercially available electrochemical sensors, which have sensitivity of over tens of ppb."

NH_3 sensitivity was of the order of tens of parts per billion (ppb). "The responses to NO_2 and NH_3 are in the opposite directions, corresponding to p-doping by NO_2 and n-doping by NH_3," the team reports.

"This sensor could be used in a compact device that could measure NO_2 anywhere, in real time, at the environmental benchmark level of sensitivity of 40–60ppb, which is an index of air pollution," Fujitsu adds.

Although the device was sluggish to return to its original performance when exposed to pure carrier gas (nitrogen), the researchers believe that heating the sensor could speed re-setting. "In practice, this sensor should be used at relatively high operation temperature, which is a strategy often employed in commercial sensors."

Fujitsu has already developed a sensor for NH_3 based on copper bromide p-type semiconductor material that, combined with the graphene sensor for NO_2, could result in "a highly sensitive and portable sensor that can be used as conveniently as a thermometer to measure gases in human breath for early detection of lifestyle diseases".

Nanotubes

IBM T.J. Watson Research Center presented end-bonded contacts to carbon nanotubes (CNTs) created through a low-temperature process [session 5.1]. The contacts were used to fabricate both p- and n-channel field-effect transistors (P-/N-FETs).

CMOS inverters based on CNTs with end-bonded contacts are claimed as demonstrating the smallest contact size thus far for such circuits. The team hopes that the technology could pave the way to realizing CNT-based scalable CMOS technology.

The semiconducting CNTs were deposited on a 10nm

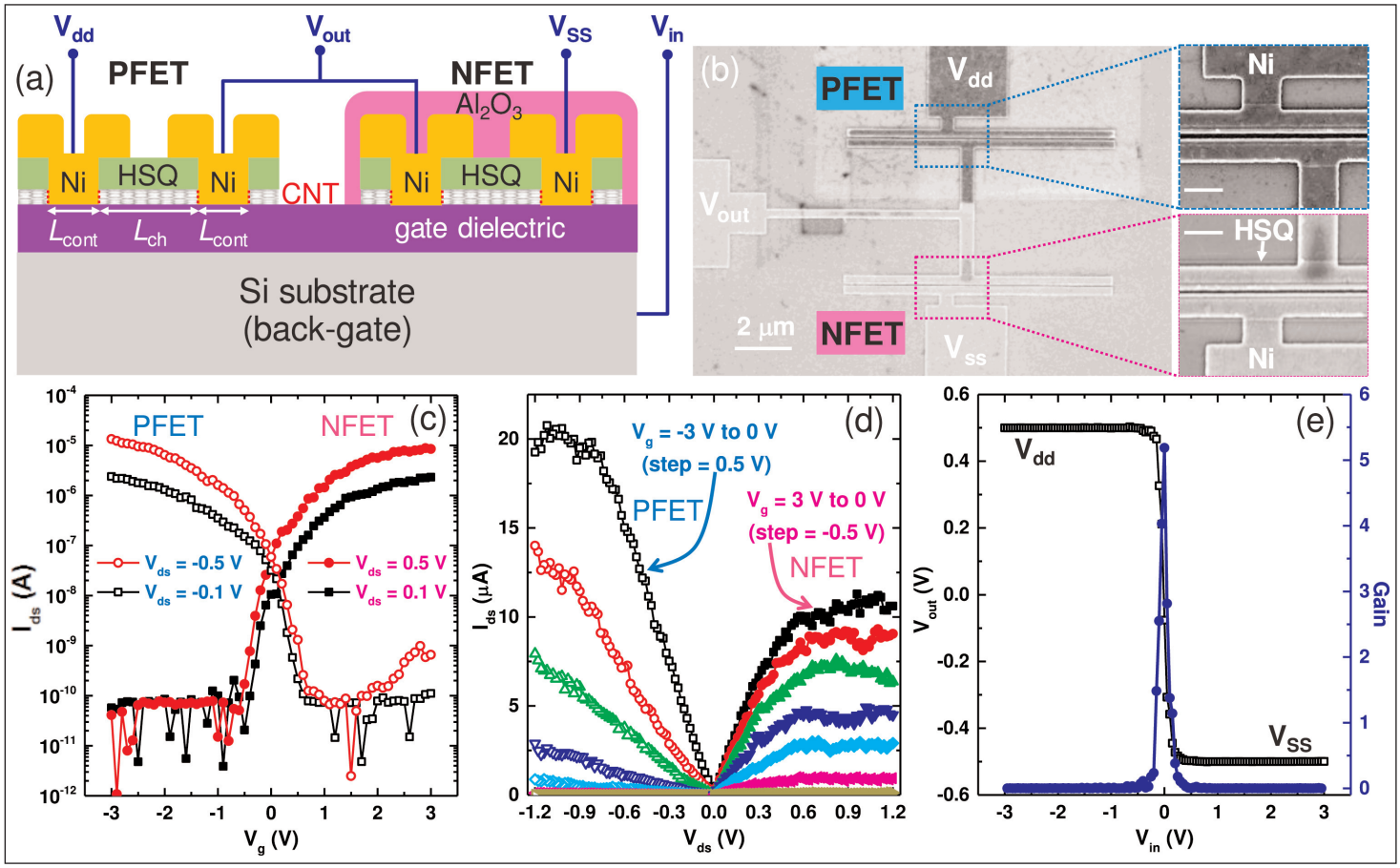

Figure 6. (a) Schematic of CNT-based CMOS inverter with entirely Ni end-bonded contacts. (b) SEM images of CMOS inverter with nominal 150nm channel and 40nm contact lengths. Insets' scale bars 400nm. (c) FET drain currents (I_{ds}) versus (c) gate potentials (V_{gs}) and (d) drain biases (V_{ds}). (e) Output voltage (left axis) and inverter gain (right axis) as function of input voltage.

SiO_2 layer on silicon substrate. Without annealing, fabricated back-gate transistors demonstrated ambipolar behavior with less than 1μA on-current. Annealing in the 400–600ºC range converted the transistors to unipolar p-type performance with an on-current of ~10μA.

"Such a dramatic transition upon annealing hinted at a transformation in the contact scheme, that is, from Ni side-bonded contacts to end-bonded contacts," the researchers comment. The team also suggests that the end bonding is due to carbon dissolution into the metal.

The on/off current ratio was near to 10^6 with a peak transconductance of 3.1μS. The contact resistance was relatively size-independent at around 30kΩ. This is taken as indicating end-bonding rather than the usual side-bonding.

Palladium contacts had a similar performance boost on annealing, but nickel (Ni) contact devices showed less variations in operation characteristics. Apart from the better reliability, Ni is preferred in terms of cost and reduced contamination of existing silicon-based production lines.

Atomic layer deposition (ALD) of 20nm aluminium oxide (Al_2O_3) converted the transistors to n-type performance. Hydrogen silsesquioxane (HSQ) trenches defined the contact regions and protected the CNT channel.

"The mechanism for the observed PFET-to-NFET conversion could be attributed to electron doping in the CNT from the fixed charge in the Al_2O_3 layer and also the electric dipole formation at the Al_2O_3/HSQ interface," the researchers suggest. This allowed the researchers to demonstrate CMOS inverter circuits with gain higher than 5 using PFET and NFET structures (Figure 6).

Since Ni is ferromagnetic at room temperature, the researchers also believe that spintronics could be used to add more functionality in future CNT-based devices and circuits.

Researchers from South Korea and USA claimed the first demonstration of a wrap-gate CNT-FET with vertically suspended channels [session 5.2]. The team from Korea Advanced Institute of Science and Technology (KAIST), Kookmin University, NASA Ames Research Center, and South Korea's National Nanofab Center reported enhanced gate controllability and charge transport capabilities. The CNT channels were deposited on a silicon nanowire frame, followed by source/drain and all-around gate formation with Al_2O_3 dielectric and atomic layer deposition Ni electrode (Figure 7).

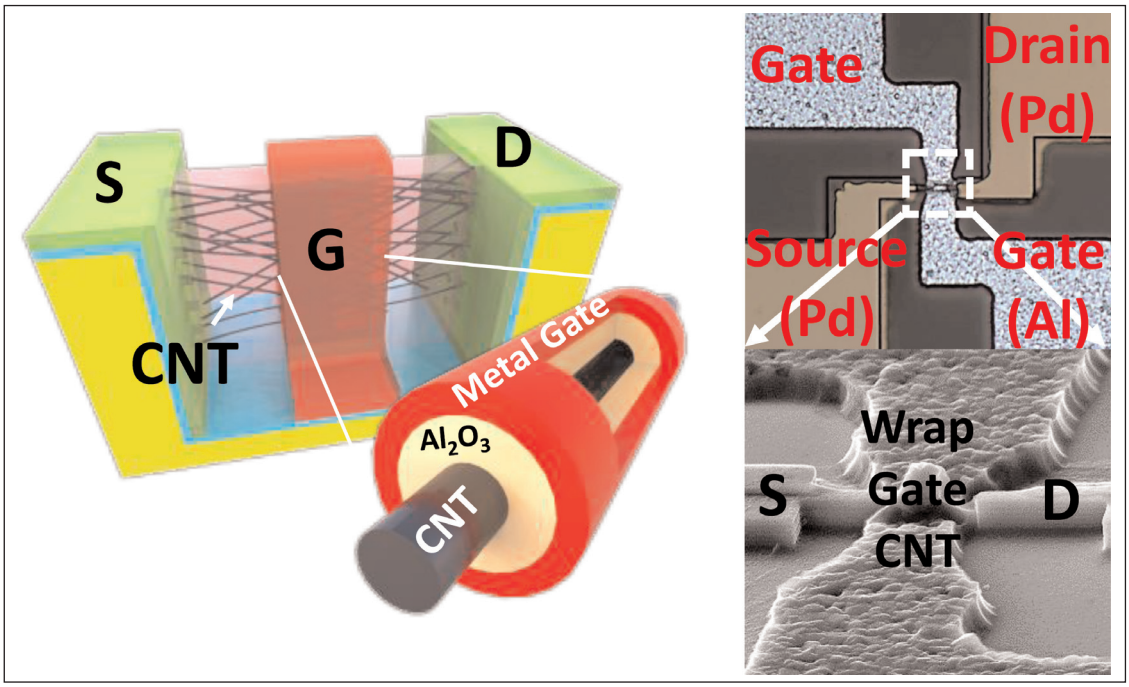

Figure 7. Gate-all-around CNT FET.

Transition-metal dichalcogenides

Stanford University claimed record saturation current for its monolayer molybdenum disulfide (MoS_2) transistors with self-aligned 10nm top gates (SATFETs) [session 5.6]. The current was more than 400μA/μm.

MoS_2 is one of a range of 'transition-metal dichalcogenide' compounds that are layered at the atomic level. The layers can be separated in a similar way to graphite/graphene. An alternative transition metal is tungsten, while tellurium or selenium can be used for the dichalcogenide.

The Stanford MoS_2 SATFET also achieved sub-threshold slopes as low as 80mV/decade. The equivalent oxide thickness (EOT) was reduced to 2.5nm is some devices.

The device was produced by CVD on SiO_2/Si substrate. A monolayer of MoS_2 is 0.615nm thick. The gate was built by depositing a 2nm seed layer of Al that was allowed to fully oxidize in air. A thicker layer of Al was added to form the gate and a 5nm self-passivated surface oxidation layer around the entire electrode.

A 10nm gold (Au) layer covered the entire structure that was used to create self-aligned source and drain electrodes. Thicker titanium/gold (Ti/Au) metalization was used to create electrodes away from the channel. The device had a ~10nm gate length with 5–6nm gate oxide thickness.

The researchers also report 0.25 ballistic transport transmission at low temperature. Normally charge carriers will suffer a number of scattering events between the source and drain of a transistor. Reducing the amount of

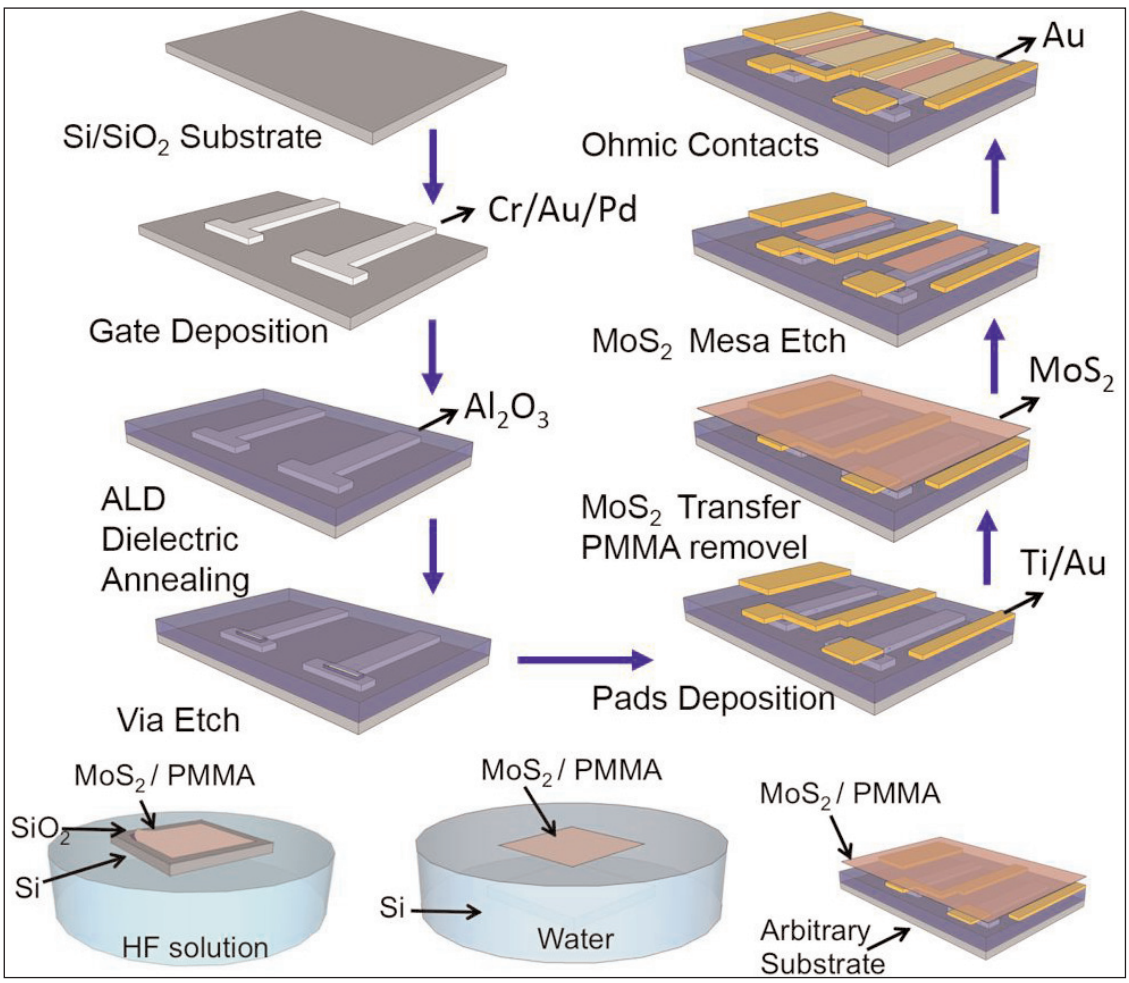

Figure 8. Overview of fabrication steps.

scattering increases conductivity in the channel. Ballistic transport describes the limit where the number of scattering events goes to zero. The researchers report: "Combining modeling and measurements, we examine diffusive versus ballistic transport and suggest a route to advance MoS_2 transistors closer to the ballistic limit."

Massachusetts Institute of Technology (MIT) and Taiwan National Tsing-Hua University is looking towards realizing high-yield large-area MoS_2 circuits with a view to co-optimization of materials, devices and circuits through a variation-aware design flow and yield model [session 5.7]. The team fabricated test chips with various inverters and basic logic gates (such as NAND and XOR) with close-to-unit yield (Figure 8).

Zhejiang University has used MoS_2 as a capping layer for germanium (Ge) quantum well channel CMOS devices [session 33.3]. GeO_2 does not easily form a stable passivated interface on Ge. Epitaxial silicon can be used for pMOS but not nMOS. Indium aluminium phosphide, a relatively new option, can enhance p- and n-MOS performance, but risks contamination of the Ge channel through diffusion.

The two-layer MoS_2 material was grown by CVD on SiO_2 and transferred to clean (100) Ge. The transistors were then fabricated (Figure 9). X-ray photoelectron spectroscopy (XPS) gave a 0.43eV valence band offset between the MoS_2 and Ge. Taking into account the 0.67eV Ge and 1.6eV two-layer MoS_2 bandgaps, the researchers estimate a conduction band offset of 0.5eV.

The team comments: "These results indicate that MoS_2 capping is sufficient to yield quantum well structures for both Ge p- and n-MOSFETs, to confine holes in Ge pMOSFETs and electrons in Ge nMOSFETs."

The team reports: "The MoS_2/Ge p- and n-MOSFETs exhibit drain current (I_d) twice as large as those in the Al_2O_3/Ge MOSFETs." The researchers attribute the improved performance of the relatively large devices to mobility enhancement.

Capacitance–voltage studies indicated hole and electron mobilities of 164cm^2/V-s and 161cm^2/V-s at channel carrier density 3x10^{12}/cm^2. The enhancements for MoS_2/Ge p-and n-MOSFETs were 3x and 1.5x, respectively, compared with Al_2O_3/Ge MOSFETs. The MoS_2 offsets repel holes and electrons from the relevant interface, reducing scattering effects from traps in the gate stack.

Negative-bias temperature instability (NBTI) of the pMOSFETs showed smaller threshold voltage shifts for the MoS_2 structure compared with Al_2O_3/GeO_x/Ge MOSFETs, indicating improved reliability.

Researchers at ETH Zurich using first-principles simulations of 2D semiconductor devices found that metal-MoS_2 contacts suffer from limited current injection, since carriers tend to flow at the edge of the metal layer before entering the semiconductor [session 5.4].

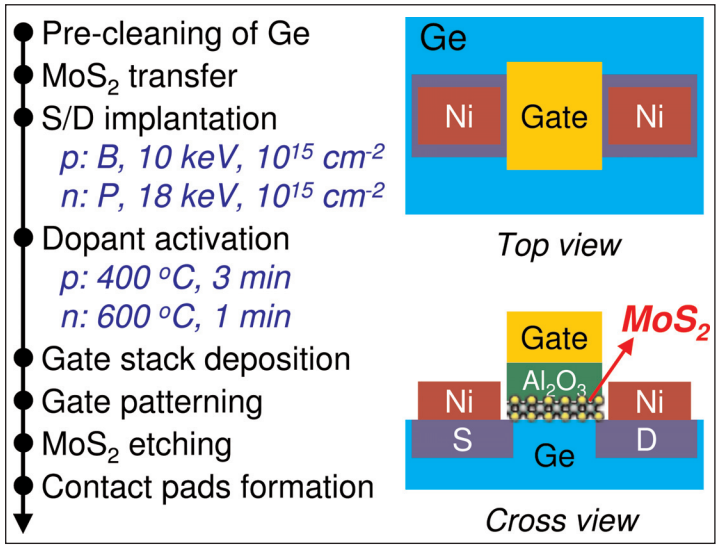

Figure 9. Fabrication procedure and device structure of MoS_2/Ge p- and n-MOSFETs.

Black phosphorus

Purdue University, Taiwan Semiconductor Manufacturing Corporation (TSMC) and US Air Force Research Laboratory reported on black phosphorus (BP) PMOSFETs with BN and Al_2O_3 gate dielectric (Figure 10) [session 5.5].

The peak transconductance (g_m) of 340μS/μm for a 200nm channel length is claimed to be the highest reported value among all BP transistors. The on-current of 850μA/μm at −1.8V drain bias and −2V gate potential is also said to be a record high. The researchers also claim record low contact resistance of 0.58kΩ-μm — "one fifth of the previous reported value of Ni/BP contact at zero gate bias", according to the team.

The sp^2 hexagonal BN (hBN) was grown on sapphire at 1050ºC by metal-organic CVD (MOCVD). BP was

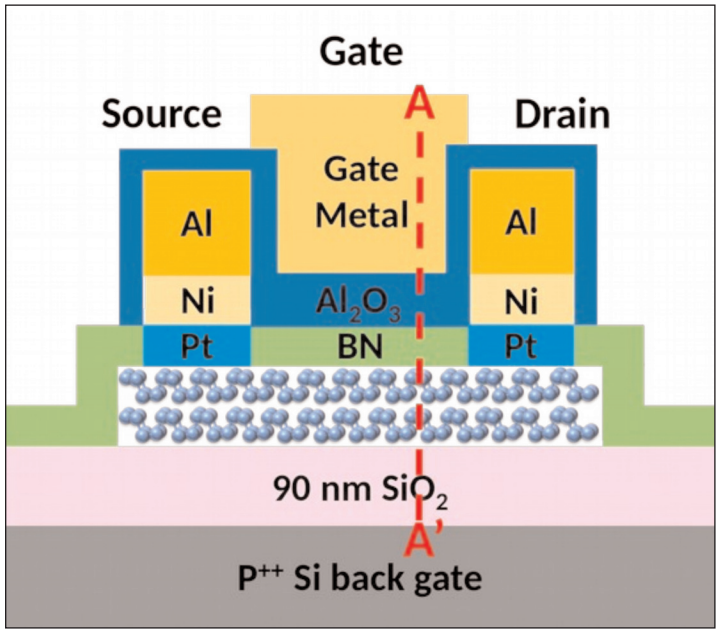

Figure 10. Schematic diagram of BP PMOSFET with BN/Al_2O_3 gate dielectric.

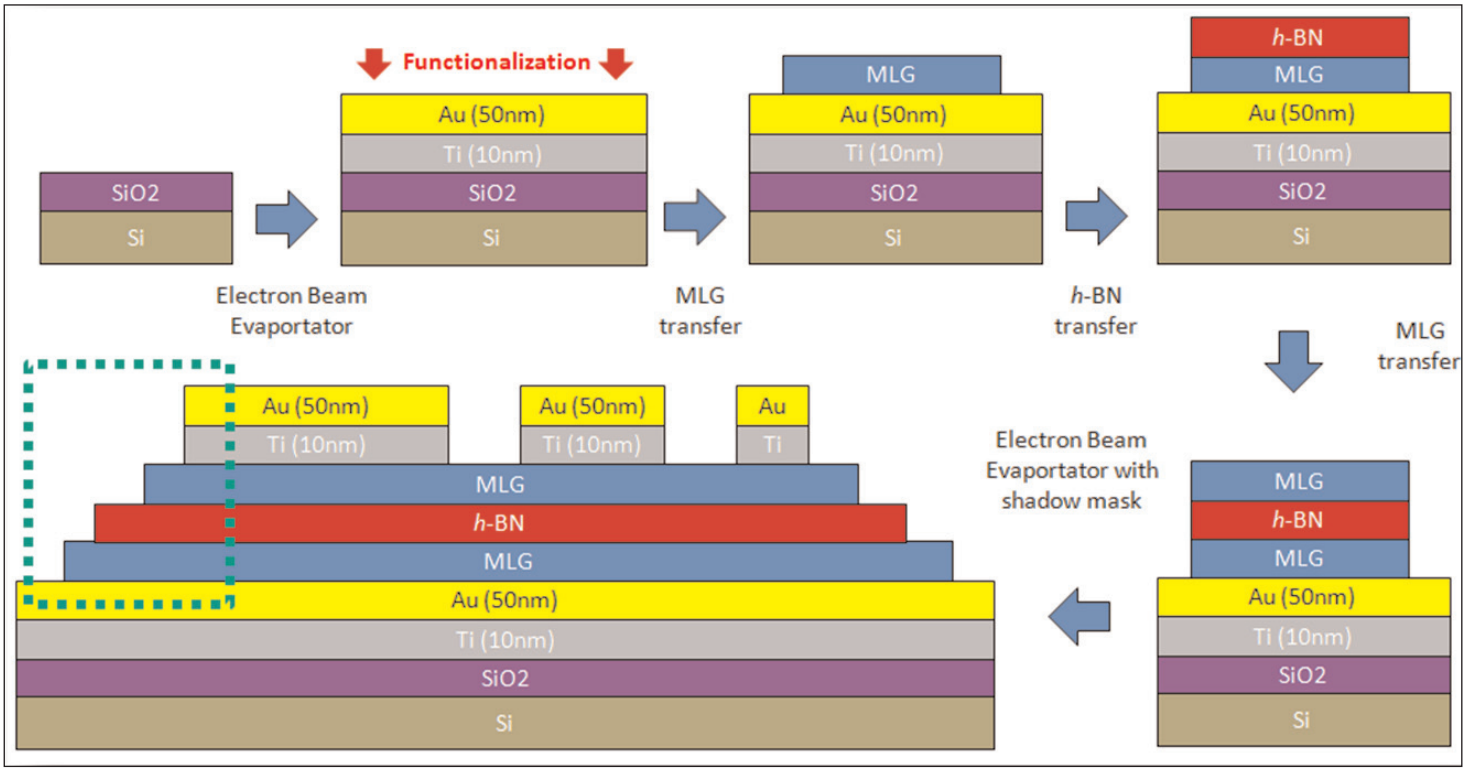

Figure 11. Fabrication flow of graphene-based samples. First, SiO_2/Si wafer is coated with Au/Ti and functionalized. Then 2D materials are transferred (sequentially), and top Au/Ti electrodes are patterned. Finally, top graphene between electrodes is removed.

produced from red phosphorus using a tin iodide/tin catalyst. BP flakes were exfoliated onto SiO_2/Si substrates. The BN was transferred onto the flakes using polymethyl methacrylate (PMMA) and polydimethylsiloxane (PDMS) coating and buffered oxide etch to peel the sapphire.

The PMMA/PDMS coating was removed and source and drain regions plasma etched into the BN before platinum (Pt)/Ni/Al (Pt) or Ni/Al metalization. The Pt/Ni/Al structure was found to have 1.6x higher on-current, compared with Ni/Al. The gate structure consisted of atomic layer deposition of Al_2O_3 dielectric and application of Ti/Au electrode.

The researchers see three factors contributing to the low contact resistance: (i) protection of the BP from oxidation by the BN; (ii) reduced interlayer resistance due to the top gate structure compared with the back gate structure; (iii) use of the high work-function metal Pt leads to a lower Schottky barrier at the BP/metal contact.

Gate leakage of the BN/Al_2O_3 bilayer gate dielectric was less than 10^{-12}A/μm^2 at –1V gate potential. The equivalent oxide thickness was 3nm. The subthreshold swing minimum was 70mV/decade.

Boron nitride

A final material with 2D properties is hBN. Università di Modena e Reggio Emilia in Italy and Soochow University in China have created resistive random access memory (RRAM) based on hBN [session 34.8].

The device consisted of 5–7 layers of BN between electrodes. One device type used metal electrodes where the BN was grown by MOCVD on copper nickel substrate and bottom electrode. The top electrode was gold on tin. An alternative device used MOCVD 6-layer graphene (G) and BN assembled on Au/Ti/SiO_2/Si wafers (Figure 11). The graphene MOCVD was performed on copper.

The metal-based devices had forming voltages between 2V and 4V. After forming, the set and reset voltages were 0.7V and –0.5V, respectively. The graphene-based RRAMs had, respectively, forming, set and reset voltages of 7–9V, 2–4V and –0.5V. The graphene-based device were more stable, along with reduced cycle-to-cycle variability. The resistive switching in G/BN/G structures suggests a mechanism based on B ions and vacancies rather than B and metal cation diffusion.

Using simulations, the researchers explain the memory behavior as arising from manipulation of B-deficient conductive filaments with cyclical release and diffusion of B ions as the key physical switching mechanism. ■

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