Atomic-layer prospects for compound semi devices

Researchers are seeking to use ALD advantages such as uniformity to enable better performance. Mike Cooke reports.

Although the principles of atomic-layer deposition have been known for some time, it is only recently that the technology has started to gain traction in production environments. Atomic-layer deposition/epitaxy (ALD/ALE) consists of sequences of pulsed precursors to build up thin films a monolayer at a time. At present, the main applications in microelectronics are for dielectric deposition (gate insulation and DRAM capacitors), transition metal nitrides, and metal films in mainstream silicon semiconductor and hard drive production.

Although there are reports from time to time of ALD of semiconductor structures such as gallium nitride quantum wells in aluminium gallium nitride barriers, the most recent uses of ALD in compound semiconductor devices are mainly of dielectric deposition for various applications. This is due to the more extensive development of these processes having already been carried out for silicon semiconductor production.

The advantages of ALD include uniformity of the layers and the atomic-level control of the resulting material structure. However, these advantages are gained at the cost of relatively slow growth rates. The growth rate depends on how fast the system can cycle through the various pulsed process steps. As one would expect from these features of ALD, the best potential for applications comes where thin but precise layers of material are needed to achieve desired properties.

While most of the present work is being carried out in the universities, some companies are also involved. In addition, the US Navy issued a call for proposals for a Small Business Innovation Research (SBIR) on 'Atomic Layer Deposition Technology for Gallium Nitride Microwave Monolithic Integrated Circuits' in December 2011 (closed in January 2012).

The aim was to develop an ALD silicon nitride (SiN) process with requirements for the resulting thin-film to be conformal, uniform, void- and pinhole-free, dense, and with no embedded traps. Further the process temperature should not exceed 300°C. The desired process would also be cost and processing time competitive compared with present plasma-enhanced chemical vapor deposition (PECVD).

In May 2012, Sundew Technologies was awarded a Phase I contract for this work. It produces ALD systems, claiming record throughput and uptime for its equipment.

Nitride HEMT passivation

In fact, many researchers prefer to use ALD to apply aluminium oxide (Al_2O_3). For example, researchers in the USA from BAE Systems and Purdue University have developed Al_2O_3 ALD as passivation for nitride semiconductor high electron mobility transistors (HEMTs) [Dong Xu et al, Electron Device Letters, published online 22 April 2013].

Nitride HEMTs allow higher-power-density and higher-efficiency amplification at high frequency. However, current collapse with pulsed signals needs to be dealt with. One technique is to add field plates that can manipulate electric fields in nitride semiconductor transistors, reducing the effect of interface traps. However, these field plates add parasitic capacitance that negatively impacts frequency and gain performance.

Another approach is to tackle the dangling bonds that create interface traps through passivation layers.

The epitaxial structure for the BAE/Purdue HEMTs was realized using metal-organic chemical vapor deposition (MOCVD) on semi-insulating silicon carbide substrates. Aluminium nitride (AlN) was used as a nucleation layer. Part of the gallium nitride (GaN) buffer was iron doped to give a semi-insulating layer below the undoped GaN buffer. The structure was completed with undoped AlGaN barrier and 2nm GaN cap.

Before the transistor formation the wafers were cleaned in acetone, methanol and isopropanol to remove organic residues and in ammonia solution to strip surface oxide layers. The Al_2O_3 layer was applied in an ASM F-120 ALD system.

The process sequence included ramp-up to 300°C and oxide self-cleaning with trimethyl aluminium (TMA). The Al_2O_3 passivation layer was built up by alternating pulses of TMA and water (H_2O) precursors in nitrogen carrier gas. The growth rate was 0.86Å/cycle.

One aim of the cleaning steps was to unpin the Fermi level by removing oxides on the epitaxial structure that can form trap states at the interface with the gate. The researchers estimate the as-grown interface trap density for their Al_2O_3/GaN cap at between 10^{11}/cm^2-eV and 10^{12}/cm^2-eV. This can be reduced to less than 10^{11}/cm^2-eV by a post-deposition anneal.

Comparison wafers were also produced with a more conventional silicon nitride (SiN) passivation applied with PECVD (250°C) and ammonia plasma pre-treatment.

The passivated material was used to create 200nm-long T-gate HEMTs with mesa isolation achieved using inductively coupled plasma etch. The ohmic source–drain contacts consisted of annealed titanium/aluminium/gold.

One effect of the Al_2O_3 layer was to reduce parasitic resistance due to the improved interface between passivation and GaN cap. This increased the 10V-drain-bias maximum drain current and extrinsic peak transconductance by 10% and 8%, respectively, over the values for SiN passivation. In addition, the subthreshold drain current was reduced by an order of magnitude in the Al_2O_3 device.

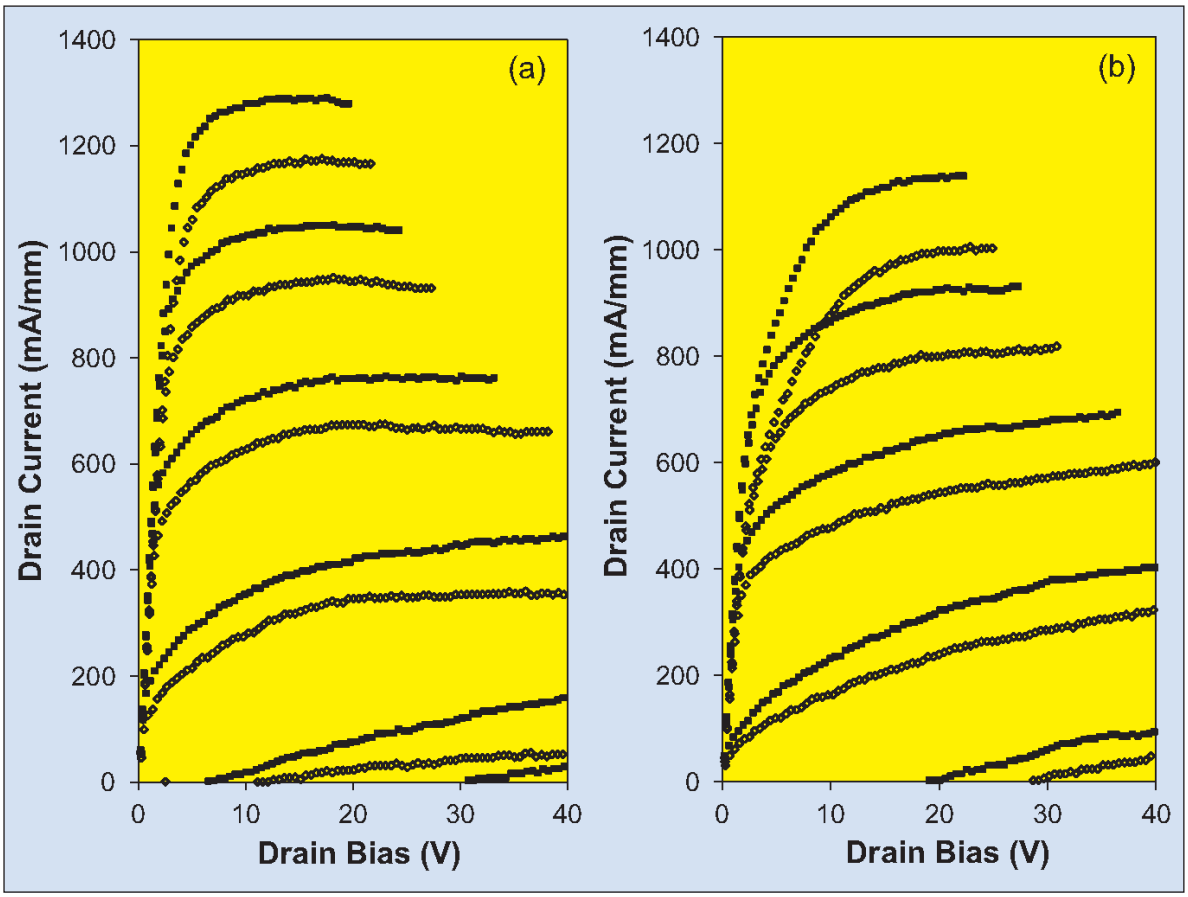

Figure 1. Pulsed current-voltage (IV) characteristics for 200nm long T-gate GaN HEMTs with PECVD SiN (open symbols) and ALD Al_2O_3 passivation (solid symbols). Devices were measured at quiescent points of (a) 0V gate and drain and (b) –5V gate and 30V drain. The gate for the top curves was 1V, and the others represent –1V steps.

The subthreshold current was attributed to gate leakage, which in the Al_2O_3 device was reduced due to the improved interface leading to better performance of the Schottky gate under reverse bias.

Performance under current pulses with 200ns width and 2ms separation was tested at different quiescent points (Figure 1). With the quiescent gate and drain bias at 0V, the maximum drain current was 10% better in the Al_2O_3 device. A 'deep' quiescent point of –5V gate and 30V drain gave an even better maximum drain current performance boost of 20% to the Al_2O_3-passivated HEMT. The pulsed performance is also more uniform across the 3-inch wafers that contain the Al_2O_3 HEMTs: the maximum current standard deviation was 11mA/mm at the zero quiescent point and 20mA/mm for the deep quiescent point, compared with 49mA/mm and 54mA/mm, respectively, for the SiN-passivated HEMT.

The researchers comment: "The improved uniformity and consistency of pulsed-IV performance with the use of an ALD Al_2O_3 passivation layer would certainly contribute to higher yield of MMIC's based on these devices, making it a more manufacturing friendly technology."

The frequency performance of the two device types was similar, with a cut-off frequency (f_T) of 54–55GHz and maximum oscillation (f_{max}) of 117–120GHz at 20V drain. However, the 10GHz continuous wave (CW) power performance (Figure 2) at 20V drain of the Al_2O_3 device was 30% better in terms of maximum output (4.55W/mm vs. 3.5W/mm). Also, the power-added efficiency (PAE) was better by about 8%. Increasing the drain bias to 25V slightly reduced the enhancement to 27% for maximum power output and 5% for PAE.

Researchers from Purdue have also worked with Harvard university, using atomic layer epitaxy (ALE) to develop gallium arsenide (GaAs) enhancement-mode (E-mode) surface/n-channel metal-organic-semiconductor field-effect transistors (NMOSFETs) with a maximum drain current of 336mA/mm, claimed to be a record high for such devices [L. Dong et al, IEEE Electron Device Letters, published online 7 March 2013; reported by Mike Cooke, Semiconductor Today, April/May, p94, 2013]. ALE and annealing of the gate dielectric reduced the density of interface traps that again kill performance by collecting charge. The charge shields the gate, reducing its electrostatic effectiveness.

The ALE dielectric stack consisted of 7.5nm lanthanum yttrium oxide ($La_{1.8}Y_{0.2}O_3$) and 6.5nm aluminium oxide

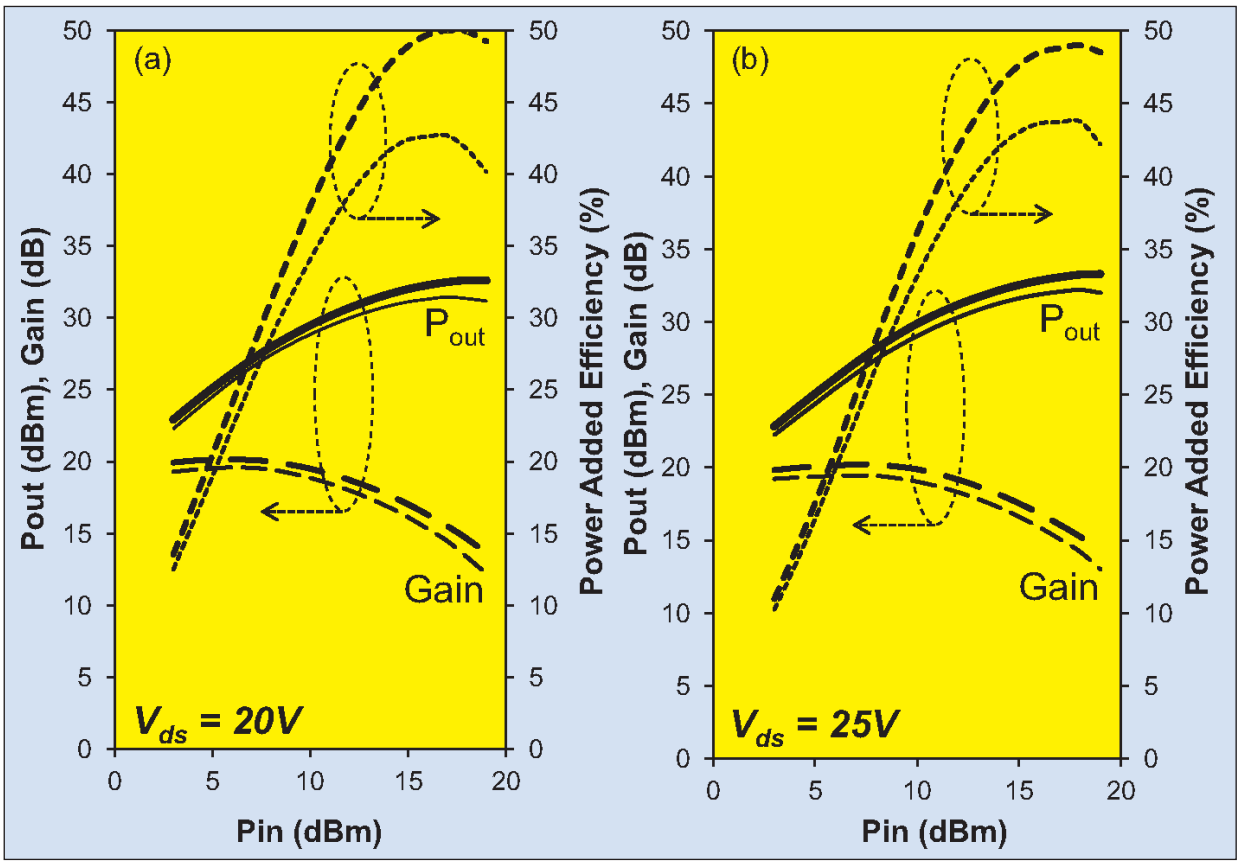

Figure 2. Output power, associated power gain, and power-added efficiency as a function of drive power for 200nm 4x100µm HEMTs passivated with PECVD SiN (thin lines) and ALD Al_2O_3 (thick lines) at 10GHz. Devices were biased at drain current of 200mA/mm and drain voltage of (a) 20V and (b) 25V.

(Al_2O_3). The Al_2O_3 was used to protect the lower dielectric layer from reacting with water molecules from the air and from the following process steps. The equivalent oxide thickness of the structure was around 4.5nm.

The researchers believe that the high quality of their novel $La_{1.8}Y_{0.2}O_3$ epitaxial interface passivates dangling bonds on the GaAs surface, reducing the number of interface traps.

Another collaboration using ALD to enhance arsenide transistor performance involved GLOBALFOUNDRIES, SEMATECH, and Massachusetts Institute of Technology (MIT) [Dae-Hyun Kim et al, IEEE Electron Device Letters, published online 4 January 2013; reported by Mike Cooke, Semiconductor Today March, p92, 2013].

In this case, ALD of 3nm Al_2O_3 gate insulator enabled indium arsenide quantum well metal-oxide-semiconductor field-effect transistor (InAs QW MOSFET) technology to achieve some of the highest and most balanced frequency performance values seen yet. Many of the improvements were attributed to the dramatically higher quality interface between dielectrics and III-V semiconductors enabled by ALD.

The gate leakage was suppressed by the Al_2O_3 insulation to less than 1nA/µm at all measured biases. This is a factor of 10^5 better than the forward bias values typical of III-V high-electron-mobility transistors (HEMTs) that depend on metal-semiconductor Schottky barriers to isolate the gate electrode.

ALD of Al_2O_3 gate insulation was also used by another team at MIT as part of an etch stop technique to improve performance of recessed-gate nitride semiconductor metal-insulator-semiconductor field-effect transistors (MISFETs) [Bin Lu et al, IEEE Electron Device Letters, published online 24 January 2013; reported by Mike Cooke, Semiconductor Today March, p90, 2013].

Gallium-doped zinc oxide

Taiwan National Tsing Hua University has reported improved modulation performance of high output power nitride semiconductor light-emitting diodes (LEDs) by using an ALD Ga-doped ZnO (GZO) transparent conducting layer [Chien-Lan Liao et al, IEEE Electron Device Letters, published online 28 March 2013].

Up to now, most research effort for visible LEDs based on indium gallium nitride (InGaN) alloys has focused on extracting higher power efficiency for white light illumination and shorter-wavelength applications.

In principle, shorter-wavelength light should enable broader bandwidths for visible light over the normal infrared of fiber optical communication. With InGaN LEDs, high power output has generally resulted in poor modulation performance.

The Tsing Hua research resulted in an InGaN LED with 225.4MHz 3dB-modulation bandwidth at 35mA injection current and 1.6mW output power. Previously high output power resulted in modulation bandwidths of tens of MHz, although at lower output powers some groups have achieved 200–330MHz.

The researchers see their device as incorporating two key technologies: the GZO current spreader and a

smaller RC constant. The GZO transparent conducting oxide (TCO) layer creates a low contact resistance while also creating a uniform near-vertical current flow through the active light-emitting layers (Figure 3). The smaller RC constant is the result of employing smaller bonding pads and rapid thermal annealing to repair damage from plasma etch processes used in fabricating the device.

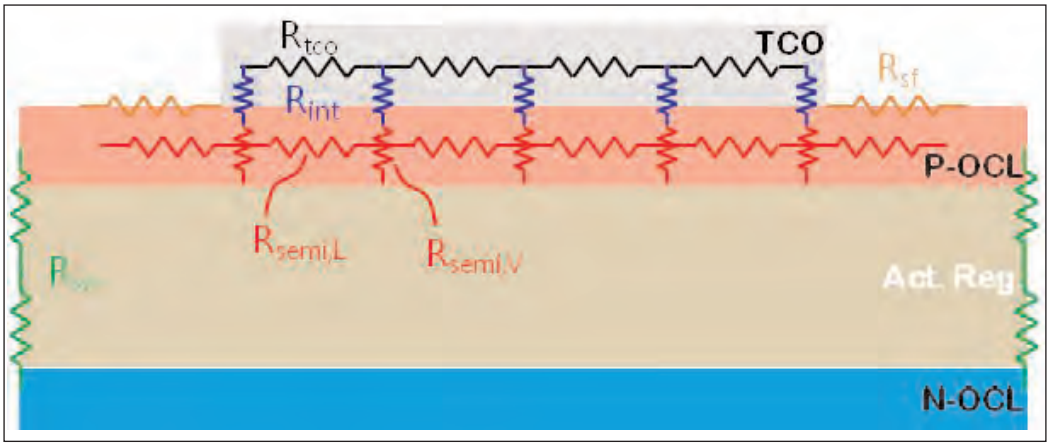

Figure 3. Resistivity optimization to create uniform near-vertical current flow through InGaN LED. This is achieved by minimizing the resistance of the TCO (R_{tco}), interface with (R_{int}) and the vertical component in the cap ($R_{semi,V}$) of the ohmic contact layer (OCL), while maximizing the resistance of the surface (R_{sf}), MQW (R_{sw}) and lateral-component for the cap ($R_{semi,L}$).

The Tsing Hua LED wafer was grown using MOCVD on sapphire (Figure 4). The undoped GaN buffer was 800nm, the n^+-GaN contact/confinement 3000nm (3μm), the p-type aluminium gallium nitride (p-AlGaN) confinement 20nm, p-GaN cap 560nm, and the n^+-InGaN contact 1.4nm. The multi-quantum well (MQW) light-emitting active region consisted of 5x 3nm InGaN wells separated by 4x 14.4nm GaN barriers.

The final 250nm GZO layer was applied using ALD with diethylzinc, triethylgallium, and water vapor precursors.

The LEDs were fabricated with ring electrodes to avoid excessive lateral current spreading. The current confined aperture was 75μm with 80μm-diameter bonding pad. The chip dimensions were 400μm x 400μm.

The sapphire substrate was lapped and polished from 430μm down to 130μm to improve its thermal conductance. Sapphire has a high thermal resistivity, which can cause problems with thermal management. Reducing the heat transport distance across sapphire was aimed at tackling this.

The peak wavelength of the device was ~441nm, although there was some blue-shift to shorter wavelengths at high current injection due to energy level shifts in the MQW as electric fields are applied (quantum-confined Stark effect). The capacitance of the device under reverse bias was low at ~2pF on average. The capacitance of the bonding pad was also reduced by using relatively low dielectric constant silicon dioxide as insulator. The series resistance of the device was estimated at 28Ω. The forward voltage at 20mA was 4.9V.

The researchers performed light output power and modulation bandwidth measurements (Figure 5). At 35mA, the power reached 1.6mW. The modulation bandwidth was measured as a 3dB reduction in output power (f_{3dB}) compared with the DC performance (Figure 5 inset). The bandwidth increases with injection current level. At 35mA, a bandwidth of 225.4MHz was achieved.

The researchers believe that further optimization of the confined region would increase current density and hence the bandwidth. However there are trade-offs, since increased currents tend to heat devices reducing efficiency and there are also efficiency droop effects independent of self-heating (tested using pulsed operation).

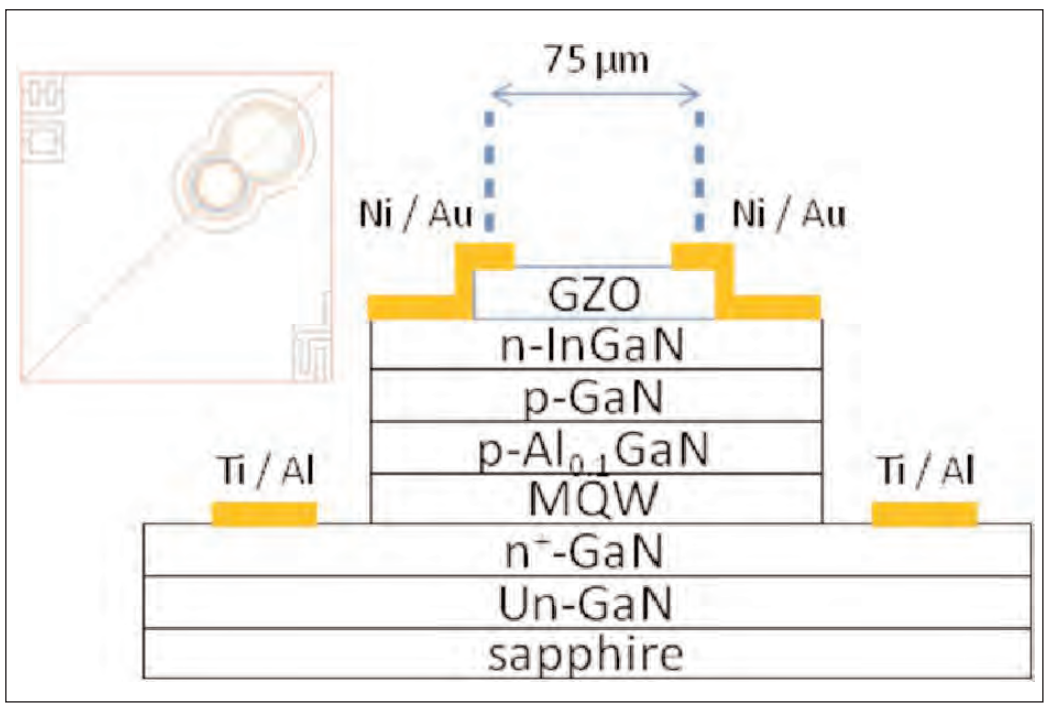

Figure 4. Epitaxial structure for blue high-speed LED. Inset: designed mask after overlapping with five steps.

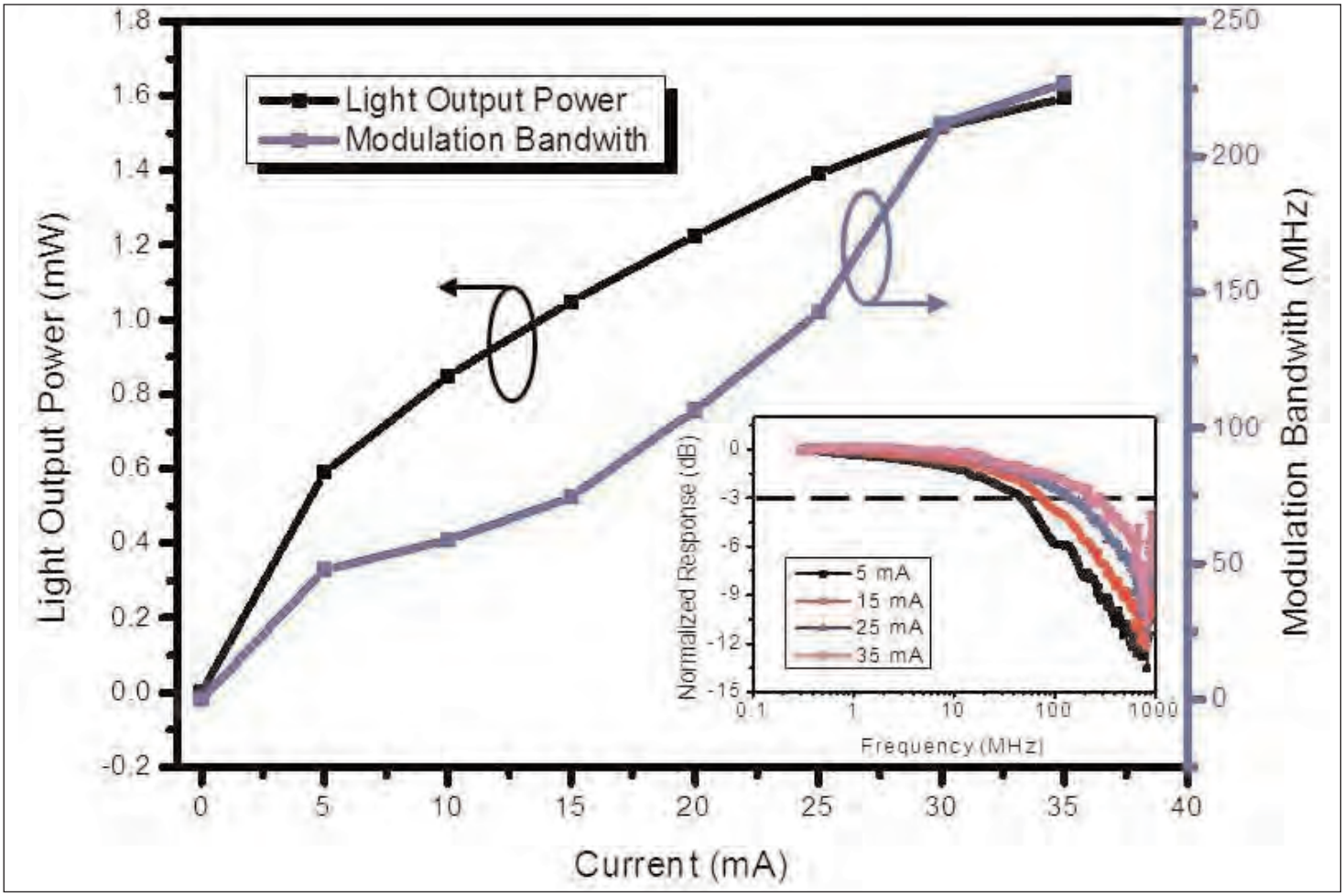

Figure 5. Light output power and 3dB frequency bandwidth (f_{3dB}) as function of forward current measured at 300K for 441nm high-speed LED. Inset: spectra of 3dB frequency bandwidth at various currents.

Efficiency droop has been ascribed to various causes such as Auger-type non-radiative recombination that kicks in at high current, polarization effects from the more ionic nature of the nitride semiconductor bond, and carriers overshooting the MQW light-emitting regions.

Finally, researchers in China have used ALD to create distributed Bragg reflectors (DBR) for increasing nitride semiconductor LED output power by up to 43% [Hongjun Chen et al, Appl. Phys. Express, vol6, p022101, 2013; reported Mike Cooke, Semiconductor Today March, p78, 2013].

Although some groups have developed DBRs for such purposes before, this is claimed as the first proposal and demonstration of DBRs grown using atomic layer deposition (ALD) rather than electron-beam (EB) evaporation. The advantages of ALD over EB evaporation include better thickness uniformity over large-diameter substrates and thickness control at the atomic level.

To develop an ALD process, the researchers from Institute of Microelectronics of Chinese Academy of Sciences and Southeast University changed the composition of the DBR from the usual titanium dioxide (TiO_2) and silicon dioxide (SiO_2) pairs to a TiO_2 and Al_2O_3 recipe. The use of Al_2O_3 also allows better adhesion of Al metal so that Al-mirror/DBR combinations can also be developed. With TiO_2/SiO_2 DBRs, an extra layer of Al_2O_3 is often applied to enable adhesion of Al-metal.

The LED wafer was back-side thinned to 100μm before the DBR and Al mirror were applied. The atomic layer deposition was preceded by soft polishing for 30 minutes to minimize the roughness of the surface. The TiO_2/Al_2O_3 DBR was designed to maximize reflectivity between 420nm and 500nm. This was achieved with 67nm Al_2O_3 and 49nm TiO_2.

The ALD used trimethyl-aluminium and water precursors for the Al_2O_3, and titanium tetrachloride and water for the TiO_2. The carrier gas was nitrogen. The growth temperature for both materials was 250°C. This enabled a reduced fabrication time and high-quality thin films. The different material depositions were separated by nitrogen purging to avoid mixing of the respective precursors.

The DBR was capped with 150nm aluminium deposited using electon-beam evaporation. Devices with TiO_2/SiO_2 (48.5nm/78.5nm) DBRs deposited using electron-beam evaporation were also produced. These were finished with a 15nm Al_2O_3 adhesive layer and 150nm Al metal.

The improvement over the traditional reflector structure was attributed to the better uniformity and thickness control of ALD compared with EB evaporation. ■