

Dynamic improvement for nitride semiconductor power switching

HRL Laboratories reduces dynamic degradation of ON-resistance in 1200V normally-off GaN-on-silicon FET to just 1.2x at 350V.

HR L Laboratories of Malibu, CA, USA has achieved low dynamic ON-resistance in a nitride semiconductor field-effect transistor with normally-OFF behavior and high breakdown voltage [Rongming Chu et al, IEEE Electron Device Letters, published online 22 March 2011]. The researchers comment: "This is the first time a 1200V normally-OFF GaN-on-Si FET with low dynamic R_{on} is reported."

HRL defined its dynamic ON-resistance as being the value attained 5 μ s after switching from OFF to ON. In its best device, HRL achieved a degradation of the ON-resistance of only 1.2x at 350V bias and 1.6x at 600V.

For power switching, the dynamic behavior needs to maintain the good performance achieved in static tests. The ON-resistance can often be degraded in high-voltage power switching from the OFF- to ON-state in nitride transistors due to field-assisted electron

trapping in the region between the gate and the drain.

In microwave nitride devices, passivation and field plates have been used to overcome this problem by reducing the effects of charge trap states. This is one reason that HRL used multiple field-plate structures to control the electric fields in its device that was designed (Figure 1) to operate at voltages much higher than those of microwave devices.

The $\sim 4\mu\text{m}$ AlGaIn epi-structures were grown on 3-inch (75mm) (111)-oriented silicon substrates using metal-organic vapor phase deposition (MOCVD). The ohmic source-drain electrodes consisted of annealed titanium/aluminum metal stacks.

The gate formation was begun with a fluorine/chlorine plasma treatment to deplete the channel electrons, providing the normally-OFF characteristic. The researchers see 'normally-OFF' operation as being

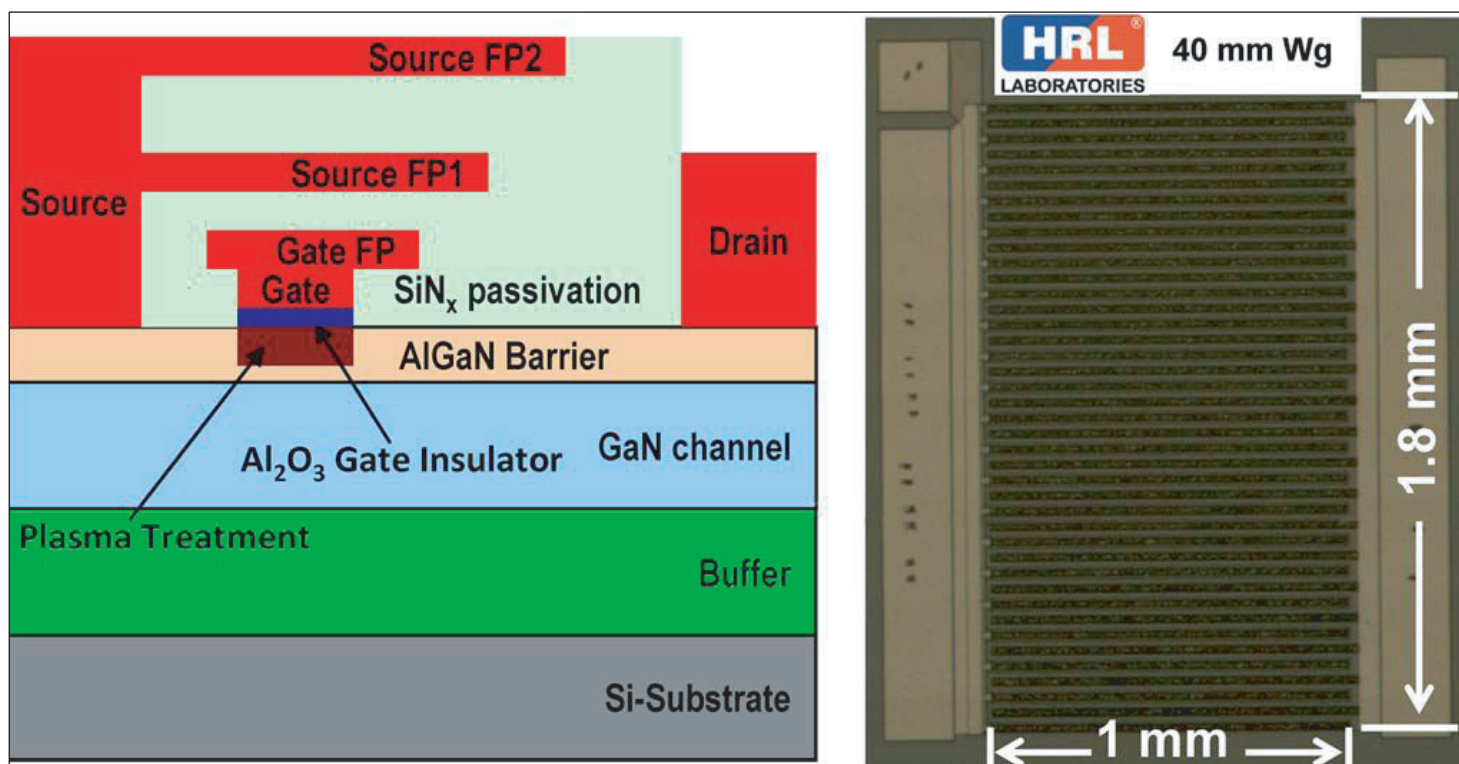


Figure 1. Cross-section schematic of device structure (left) and (right) microscopy top-view photo of GaN-on-Si FET.

particularly important for safe power switching device technology.

Fluorine is the main factor in providing the depletion and shifting the threshold voltage to positive values. Chlorine has been found to improve transconductance and reduce threshold hysteresis.

The hysteresis factor is caused by charge traps that occur near insulator–semiconductor interfaces, particularly in III-V devices. When there is a large gate bias swing expected in operation, hysteresis must be minimized for stable operation.

HRL's device has a gate dielectric/insulator of Al_2O_3 , applied using atomic layer deposition (ALD). The $1\mu\text{m}$ -length gate was completed with a nickel-gold electrode.

A silicon nitride passivation layer was grown using plasma-enhance chemical vapor deposition (PECVD), then the field plates were added — one to the gate and two to the source electrode.

The completed devices had a gate width of 40mm and an active area of 1.8mm^2 . The dies were attached to transistor outline TO-257 metal packages. The source terminal and silicon substrate were bonded to the metal can, while the gate and drain electrode were bonded to the input and output leads.

Process control monitor (PCM) devices were also processed on the wafers. A low threshold hysteresis of 0.1V was measured in these devices, indicating a low interface charge trap density.

Within a gate bias range from -3V up to $+3.5\text{V}$, the maximum drain current at 5V drain bias was $0.18\text{A}/\text{mm}$ and the gate leakage was of the order of $10\text{nA}/\text{mm}$. The researchers see low gate leakage as being important for high breakdown voltage, reduced power wastage, and simplified gate drive design.

HRL defined the threshold voltage (V_{th}) as being the gate potential at which the drain current reaches $1\mu\text{A}/\text{mm}$ at 5V drain bias. In these terms, some 600 PCM devices were tested and found to have 0.64V threshold on average with standard deviation 0.04V . The researchers comment: "The good uniformity of the

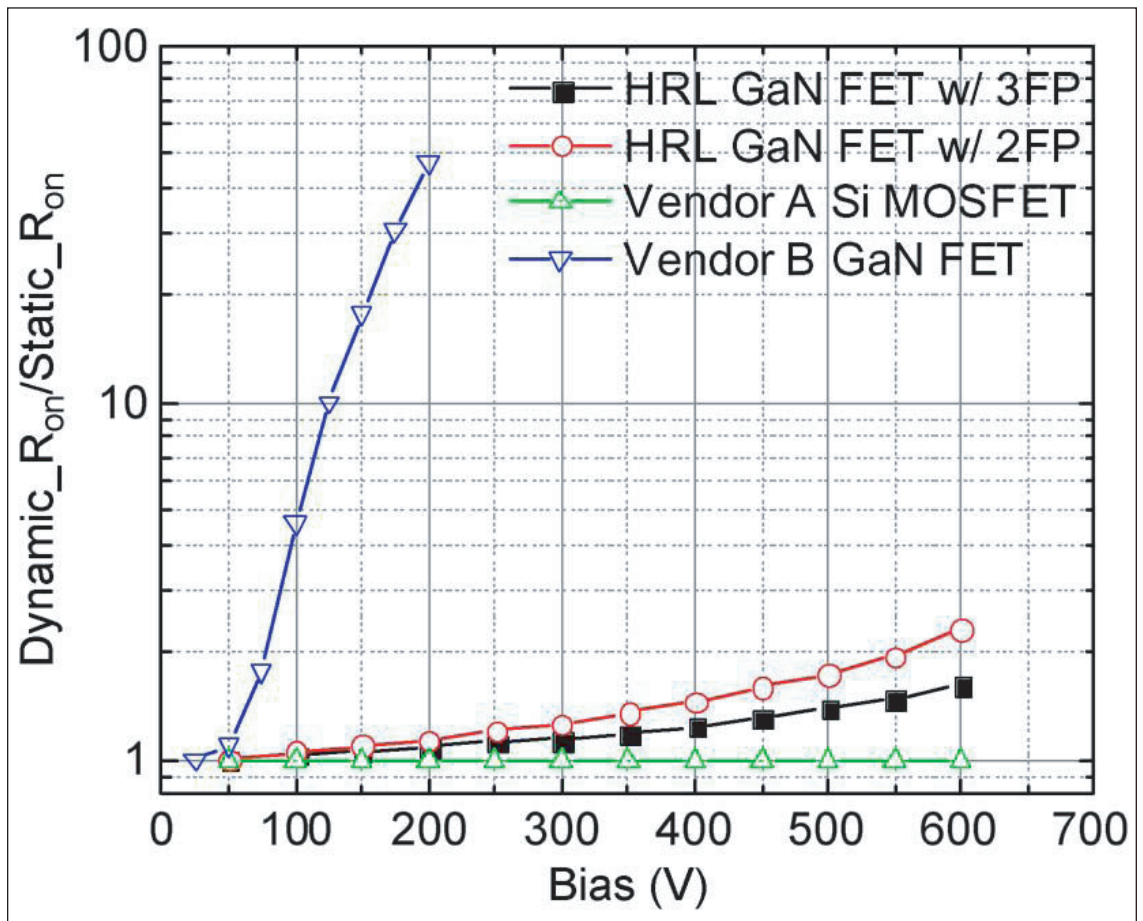


Figure 2. Ratio between dynamic ON-resistance and static ON-resistance at varied operating biases for different devices.

V_{th} of the PCM devices suggests the feasibility of constructing normally-OFF FETs with large gate width, as well as the manufacturability of our device fabrication process."

The static ON-resistance of a packaged device was 0.5Ω or $9\text{m}\Omega\text{-cm}^2$ at a gate potential of 3V and a drain current of 2A . The catastrophic breakdown at zero gate potential (OFF) was 1200V . The researchers comment: "The low R_{on} and high breakdown achieved with this device make it a very competitive candidate for high-voltage power-switching applications."

HRL compared its device (Figure 2) with varying numbers of field plates, along with commercial silicon superjunction power MOSFET and nitride FET devices. The silicon device showed no dynamic degradation of ON-resistance. The HRL FET with three field plates suffered some degradation of $1.2\times$ at 350V bias and $1.6\times$ at 600V . The researchers comment: "This is, to our knowledge, the best dynamic R_{on} performance achieved for a normally-OFF GaN FET on Si substrate."

The HRL team believes that further optimization of the field-plate configuration and epilayer quality could improve these dynamic characteristics towards a degradation-free level. ■

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