Exploring CMOS power amplification for mobile phones

Qualcomm has announced a CMOS radio-frequency front-end solution for mobile phones, including a CMOS power amplifier. How close is silicon to compound semiconductors for this application? Mike Cooke reports.

Recently the prospect has been raised that silicon could kick compound semiconductors out of the radio front-end of mobile phones in the near future. This has already been partially accomplished with the move to antenna switching and tuning technologies based on silicon-on-insulator (SOI) devices.

A further shot across the bow is Qualcomm's announcement of its RF360 'front-end solution', consisting of a dynamic antenna matching tuner (QFE15xx), envelope power tracker (QFE11xx), integrated power amplifier/antenna switch (QFE23xx), and RF 'POP' (QFE27xx).

The QFE23xx is claimed to be the industry's first chip that integrates a CMOS power amplifier (PA) and antenna switch with multiband support across 2G, 3G and 4G LTE cellular modes. This is a real concern for compound semiconductor manufacturers, since much of their financial prosperity has been based on the supply of power amplifiers for mobile phones.

Qualcomm expects OEM products featuring the complete solution in second-half 2013. The trademarked 'POP' device is a '3D package' consisting of the QFE23xx PA/switch, along with filters and duplexers in a single component.

The use of CMOS, according to Qualcomm, has been enabled by its modem-assisted envelope tracking technology, which is designed to reduce the overall thermal footprint and RF power consumption by up to 30%. Qualcomm points to a smaller PCB area and simplified routing as attractions for its solution.

Although silicon is well established in the high-frequency PA market for nearer-range products such as Bluetooth and WiFi, the material faces a real challenge in supplying the signal boost needed for longer-range mobile phone transmissions of up to 30km. Such distances are the worst case of a 'Macrocell', typically in rural areas. Communications in urban areas and offices can take advantage of shorter-range Microcell (2km), Picocell (200m) or even Femtocell access (50m) to reduce power drain in the phone.

Mobile networks hope to attract new business through advanced phones, but these devices set up an internal power struggle for real estate in the design, squeezing the radio footprint. Unfortunately, the problem has been worsened by new network standards such as Long-Term Evolution (LTE) with their proliferation of possible frequency bands ('fragmentation'). In addition, the newer radio technologies require the PAs to run in a more linear fashion, reducing power efficiency.

The old methodology of having a series of narrow-band PAs dedicated to each frequency range is no longer adequate. In the past few years, PA manufacturers have been rolling out various multi-mode multi-band (MMMB) PA solutions designed to meet this challenge.

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Although the RF components have increasingly been packaged in modules, the industry would like even more integrated solutions. Separate compound semiconductor PAs are not easy to integrate within a silicon framework. This may change as a result of extensive work in integrating compound semiconductor high-mobility channels on silicon substrates to allow further CMOS scaling. However, such a solution will not be available for some time and, up to now, separate compound semiconductor PAs have been the only technology to deliver the required power densities for all but the lowest end of the mobile phone market.

Looking at the present typical RF front-end module (RFFE, Figure 1), there are two obvious directions to

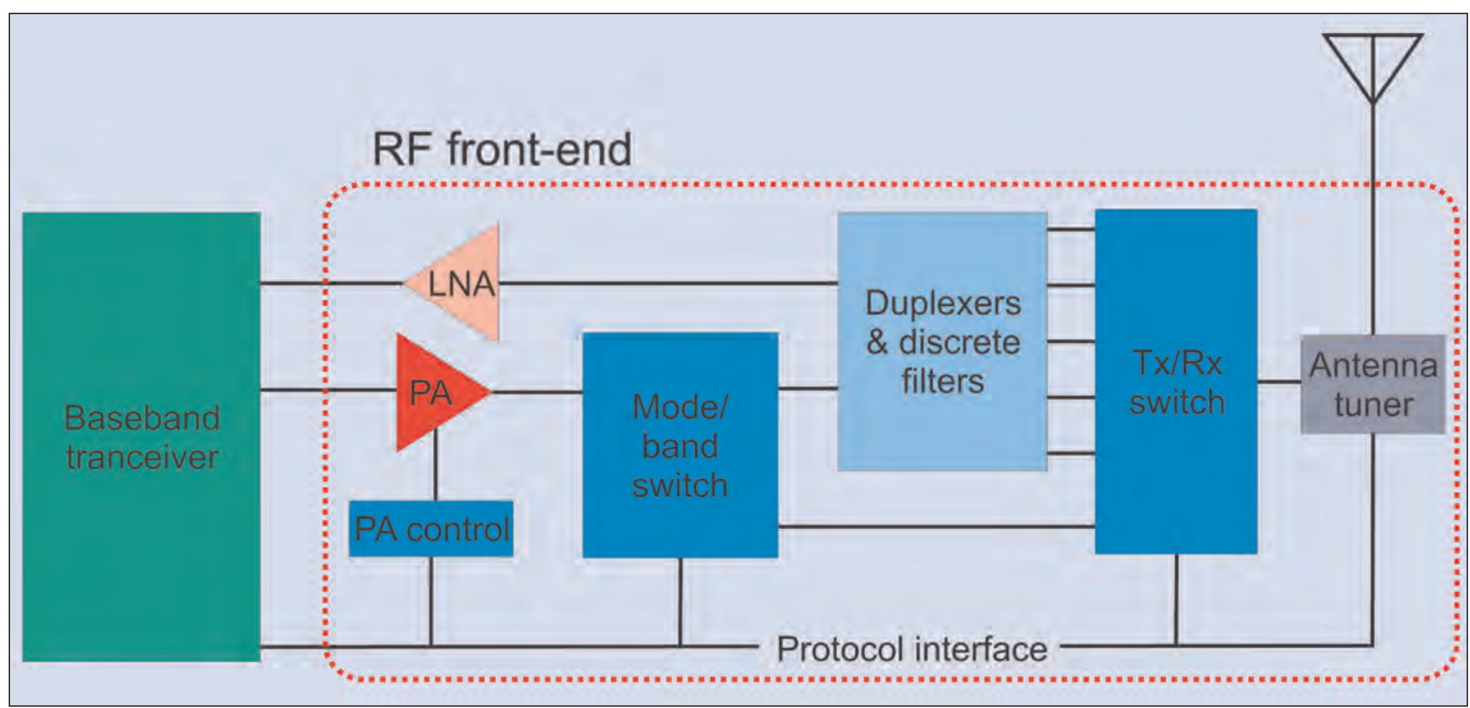

Figure 1. Block diagram of RF front-end module, including power amplifier (PA) and low-noise amplifier (LNA) and other components necessary for transmit (Tx) and receive (Rx) functions on signal from baseband transceiver.

integrate: PA+antenna switching/tuning or PA+power management. As was seen above, Qualcomm has adopted the first of these options. Since recent antenna switching/tuning components are generally based on silicon-on-insulator (SOI) technologies, it would not be surprising to learn that the Qualcomm chip is based on such an approach. Indeed, many commentators have speculated that this is the case, although Qualcomm has not confirmed this so far.

CMOS power management integrated circuits generally combine amplifier power level and mode control, bias management, dc-to-dc converter, power regulators, and electrostatic discharge (ESD) handling. These devices can also include more complex RF modulation features such as envelope tracking. CMOS is the favored technology for this due to its combination of high performance with low cost.

SOI substrate manufacturers IQE and SOITEC are hoping that the application in RF PAs could lead to increased business on top of the already successful antenna switch/tuning market. Theoretically, SOI CMOS offers better frequency response, high-perform-

Block	Key device parameter	Key substrate parameter	2011 market technology of choice
Switch	Breakdown voltage, R_{on}, RF loss	Linearity, resistivity	GaAs pHEMT, SoS, HR-SOI
Power amplifier (PA)	Gain, f_T, current density, breakdown voltage	Carrier mobility, thermal dissipation, linearity, resistivity	GaAs HBT, LDMOS
Power mgt unit (PMU)	R_{on}, current density, breakdown voltage, CMOS enable	Thermal dissipation	HV CMOS
Filter	Q(L), temp stability, coupling coefficient	Resistivity, piezoelectricity	SAW, BAW , IPD, smd

Figure 2. SOITEC's 2011 view of RFFE technologies.

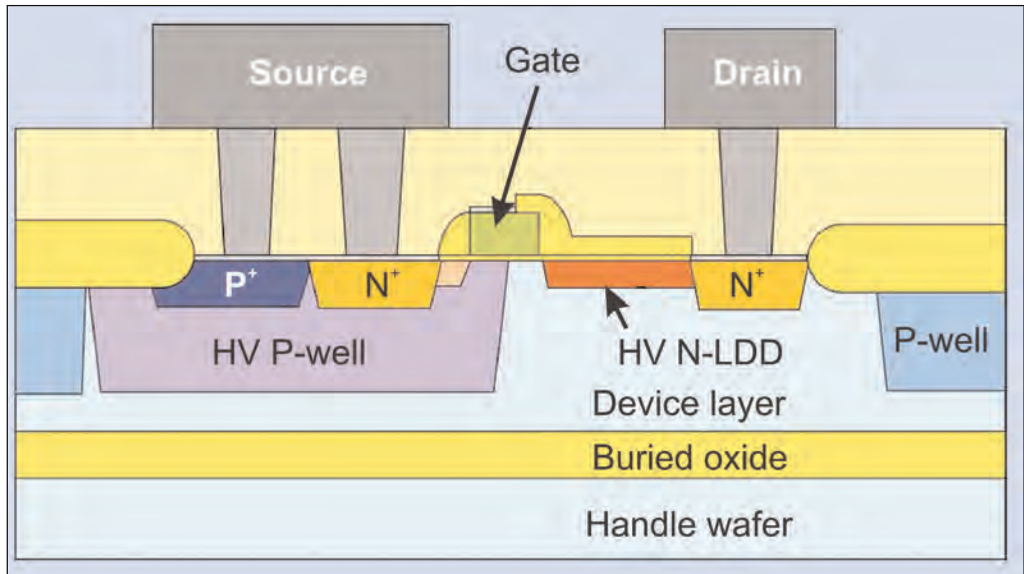

Figure 3. RFMD's IPMOS high-voltage (HV) power device on 1000Ω-cm resistivity SOI substrate. Device incorporates lightly doped drain (LDD) extension. The same structure was also produced on bulk silicon substrate of 3Ω-cm resistivity.

ance passive components, and better isolation, compared with standard bulk CMOS.

Silicon-on-sapphire (SoS) is a particularly attractive SOI technology. According to a white paper by Soitec's Eric Desbonnets and Stéphane Laurent [RF Substrate Technologies for Mobile Communications, May 2011, www.soitec.com/pdf/RF_SubstratesTechnologies_2011-07-07.pdf]: "SoS substrates are well recognized for delivering the best-performance switches. As shown in Figure 2, this material has all the performance attributes needed for RFFE module integration, combining power amplifiers, switches and antenna tuning on a single chip."

High-resistive silicon-on-insulator (HR-SOI) is a similar technology that could also be used for full RFFE module integration, including multiple functions on one chip. Desbonnets and Laurent add: "HR-SOI combines the extremely good performance of SOI for isolating signal from noise while ensuring signal power integrity. It also shows a good insertion loss and brings the same programmability level as a standard silicon bulk substrate."

Table 1. RFMD IPMOS device parameters on bulk silicon and SOI substrates.

Parameter	Bulk-Si	SOI
Threshold voltage, V_{TH} (V)	0.95	0.95
Saturation drain current, I_{DSAT} (mA/mm)	500	460
Max. g_m, (mS/mm)	145	140
Drain source breakdown voltage, BV_{Dss} (V)	18	18
ON Resistance, R_{ON} (Ω-mm)	2.8	2.8
Leakage Current, I_{OFF} (nA/mm)	0.5	0.5
fT/f_{max} (GHz)	21/40	21/42

One successful SoS antenna switch/tuning supplier, Peregrine Semiconductor, has also been exploring the integration of PAs into its process. The latest Peregrine SoS 'UltraCMOS' process is its Semiconductor Technology Platform 8 (STeP8), which uses a 250nm process that gives a 40% die shrink compared with its STeP5. Among the improvements claimed is a 36% reduction in the on-resistance/off-capacitance product.

The firm has recently transitioned from being a manufacturer with a foundry service to becoming a fabless supplier. In 2010, Peregrine entered an exclusive agreement to develop UltraCMOS with IBM using 180nm technology. This year, Peregrine also made a sourcing arrangement with Murata Manufacturing Company of Japan. This allows the Japanese company to buy or manufacture RF switches based on Peregrine's technology for RFFE modules.

Another company that produces products based on Peregrine's technology is MagnaChip of Korea, which expanded its arrangement to STeP5 late last year. Other SOI RF switch producers include Honeywell, Skyworks and TowerJazz.

Another CMOS-SoS PA development was reported last year by University of California San Diego (UCSD) with a device boasting 50% overall power-added efficiency (PAE) and 29.3dBm output power [M. Hassan et al, IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), 2012]. The process technology for the PA was 0.35μm, while an associated envelope-tracking amplifier was produced using 0.18μm bulk CMOS.

RF Micro Devices Inc (RFMD) has also been researching silicon PAs for the cellular market [Ali Tombak et al, IEEE Transactions On Microwave Theory and Techniques, vol. 60, p1862 2012], although presently most of its products are compound semiconductor based. The RFMD work includes attempted integration with power management circuitry.

The RFMD researchers used a 0.5μm high-voltage CMOS process on bulk and SOI substrates (Figure 3). The fabrication process is already a standard one for producing PA power controllers. The n-MOSFETs and p-MOSFETs are rated 5V and feature a gate with 130Å oxide insulation and silicided polysilicon electrode. The structure for the 'integrated power MOS' (IPMOS) transistors is a variant of laterally diffused MOS (LDMOS) transistors, as used for

Table 2. Comparison of RFMD IPMOS PA with other technologies. Last column is RFMD's RF3158, quad-band GSM/EDGE/GSM850/EGSM900/DCS/PCS power amplifier module.

Technology	RFMD IPMOS SOI LDMOS	Si CMOS	Si LDMOS	SiGe HBT	RFMD GaAs HBT
PCS P_{out}/PAE (dBm/%)	**3.5**	3.5	3.5	3.4	3.6
V_{DD}/V_{CC} (V)	**35.6/62**	35/51	34/50	34.5/55	35/50
GSM 900 P_{out}/PAE (dBm/%)	**33.4/47**	33/45	32/47	32.5/45	33/49

base-station PA applications.

An important difference from standard LDMOS is that the heat dissipation is through copper pillar flip-chip packaging rather than through the handle wafer. The packaging also includes optimal ground inductances for the PA. Using the packaging rather than the substrate for grounding also allows the use of SOI. The resistivity of the SOI was 1000Ω-cm, compared with 3Ω-cm for the bulk silicon. The epitaxial silicon layer on the insulation was thicker than 1μm.

DC and RF measurements (Table 1) show little difference in performance. The lower saturation current and transconductance for the SOI device are attributed to self-heating effects arising in the wafer-level measurements. The actual differences in saturation drain current and transconductance for packaged SOI products using a copper pillar flip-chip are expected to be negligible, the researchers say. The small increase in the maximum oscillation frequency is attributed to reduced parasitic capacitance from the use of SOI technology.

The process also allows the integration of metal-insulator-metal (MIM) capacitors with 2000pF/mm^2 density and a standard third metal layer of 3μm-thick aluminium for RF designs.

The researchers designed a three-stage PA for low- and high-band operations in the ranges 850–900MHz and 1710–1980MHz, respectively. The SOI-based PAs gave 0.2dBm better output power than bulk silicon in the low band and 0.6dBm in the high band. The power-added efficiencies for bulk-Si PAs were hit, respectively, by 4 and 6 percentage points. Compared with other technologies (Table 2), the output power for the SOI-based PA was marginally better, while the PAE was significantly higher in the low band. The advantages were degraded in the higher band.

The team comments: "The measured results are similar to commercially available GaAs-based PAs for GSM saturated PA applications, which shows that the engineered IPMOS devices can withstand typical operating conditions of saturated PAs."

The three-stage PA was also produced in a chip with integrated DC–DC buck converter (Figure 4) measuring 3.2mm x 1.9mm (converter section 1.15mm x 1.9mm). The researchers estimated the converter efficiency at 90% for output power levels greater than 25dBm. Below this output power the performance of the converter began to degrade, as is typical for such devices. By having an on-chip converter the PAE is improved by about 23 percentage points, compared with a fixed supply voltage and an output power of 25dBm at 915MHz. However, having the convertor on-chip did cause some noise problems.

Another PA manufacturer, Skyworks Solutions, actually markets a CMOS GSM/GPRS quad-band PA that is produced using a 0.13μm process. The patented technology came with the acquisition of Axiom Microdevices in 2009. The product brief talks of "improved power-added efficiency", but gives no figures. This suggests that the product as yet does not match compound semiconductor performance. ■

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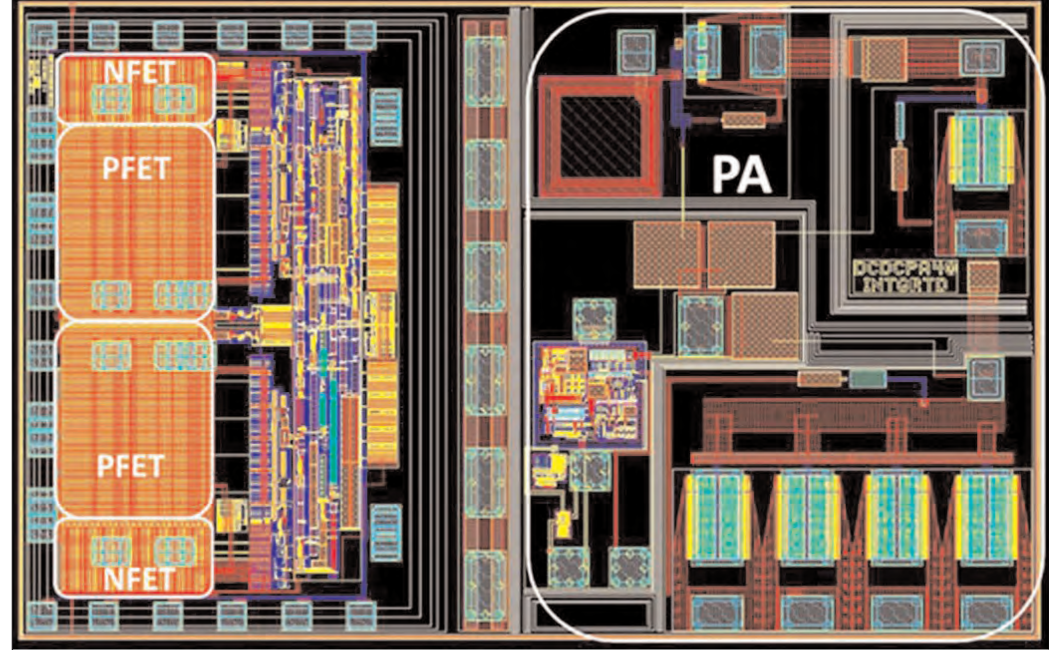

Figure 4. Layout of RFMD 3.2mm x 1.9mm integrated chip with dc/dc converter and PA.