Si implant enhances AlN spacer HEMT drain current

Japanese researchers achieve maximum current density of 1.3A/mm "competitive with other reported values for AlGaN/AlN/GaN HEMTs".

Researchers in Japan have improved the performance of nitride high-electron-mobility transistors (HEMTs) with aluminum nitride (AlN) spacers by using silicon (Si) implanted source–drain regions [Takuma Nanjo et al, Jpn. J. Appl. Phys., vol50, p064101, 2011].

AlN spacers placed between the gallium nitride (GaN) buffer and aluminum gallium nitride (AlGaN) barrier layers significantly increase the conductivity of the two-dimensional electron gas (2DEG) that is used as the channel in nitride HEMTs. However, AlN is usually highly insulating and thus makes the channel difficult to access through the source–drain regions.

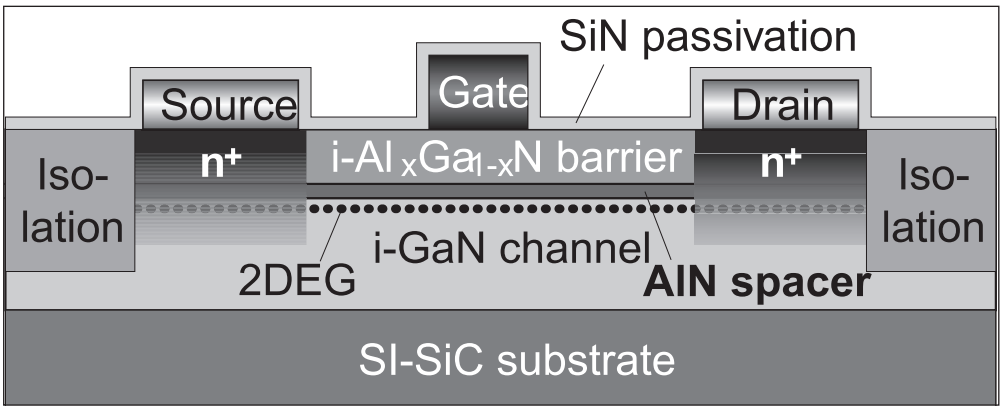

Figure 1. Schematic cross-sectional structure of AlGaN/AlN/GaN HEMT fabricated employing Si ion implantation doping.

The researchers from Mitsubishi Electric Corp and Okayama Prefectural University used Si implantation to reduce the source–drain contact resistance. They comment: "We showed a remarkable enhancement in the drain current density, which is a result of the successful combination of the use of an AlN spacer in the structure design and that of Si ion implantation doping in the process design."

The epitaxial structures with layers of GaN buffer, AlN spacer and AlGaN barrier (Figure 1) were grown on silicon carbide (SiC) substrates using MOCVD. The thickness of the buffer was 2μm, the barrier 19nm, and the spacer 1nm. Devices with 20nm barrier and no spacer were also grown for comparison purposes. Two AlGaN barriers were tested with Al contents of 20% or 25%.

The source–drain regions were formed using 50keV ^{28}Si ion implantation with a dose concentration of $10^{15}/cm^2$, followed by a rapid thermal anneal in nitrogen for 5 min at 1150°C. During these processes, the wafer was covered with silicon nitride (SiN), deposited using plasma-enhanced chemical vapor deposition (PECVD). The source–drain electrodes consisted of titanium-aluminum that was annealed for 2 minutes at 600°C.

Isolation regions were then formed using a multi-stage zinc ion implant, followed by applying the nickel-gold Schottky gate electrode. The final SiN passivation layer was applied using catalytic chemical vapor deposition.

Hall and transmission-line method (TLM) measurements were made to extract the characteristics of the 2DEG and ohmic contacts, respectively (Figure 2).

As expected, the insertion of the AlN spacer increases 2DEG carrier concentration and mobility with a 20% Al barrier. In fact, the carrier concentration is equivalent to that of a 25% Al barrier without spacer. In both cases, the increased amounts of carriers are attributed to polarization effects resulting from growing high-aluminum-content layers on the GaN buffer.

Increased Al-content of the barrier, however, reduces mobility due to alloy scattering and interface roughness effects. Insertion of the AlN spacer is effective at ameliorating alloy scattering effects in the 2DEG.

Without implanted source–drain regions, the AlN spacer yields non-ohmic contacts due to the increased potential barrier from the very wide energy bandgap of the material (~6eV). Implantation of Si created comparable ohmic behavior for all epitaxial structures, and reduced contact resistance for material without AlN spacers.

Apart from silicon being a donor of electrons in nitride semiconductors, another effect of implantation — destruction of the layer structure with indistinct boundaries being produced — was seen under scanning electron microscopy (SEM). The structure alteration of mixing the AlN with the surrounding GaN and AlGaN layers is thought to reduce the potential barrier.

The researchers comment: "Because this mixed layer structure might almost be the same as the no-spacer structure with Si ion implantation doping, similar

excellent ohmic characteristics, as mentioned before, could be obtained in spite of the AlN spacer layer insertion."

In terms of the Schottky gate, it is found that, while the reversed-bias performances were similar across the devices, the AlN spacer reduced forward currents substantially. The reduced forward current was attributed to an increased band discontinuity at the heterointerface due to polarization effects. The gate leakage in the devices without AlN spacer increased significantly above gate voltages of +3V.

Structure	Al content (x)	0.2	0.2	0.25	0.25
	AlN spacer (nm)	0	1	0	1
Hall	Sheet carrier concentration (/cm^2)	6.6x10^{12}	8:9x10^{12}	9.1x10^{12}	1.1x10^{13}
	Mobility (cm^2/V-s)	1686	1946	1546	1828
	Epitaxial sheet resistance (Ω/sq)	558	357	443	306
TLM	Epitaxial contact resistance (Ω-cm^2)	5.9x10^4	Non-ohmic	7.0x10^4	Non-ohmic
	Implanted contact resistance (Ω-cm^2)	1.4x10^6	1.1x10^6	1.7x10^6	2.4x10^6
	Implanted sheet resistance (Ω/sq)	215	251	251	269
HEMT	Source resistance (Ω-mm)	0.95	0.77	0.90	0.83
	Measured maximum transconductance (S/mm)	0.21	0.22	0.21	0.22
	Intrinsic maximum transconductance (S/mm)	0.27	0.26	0.26	0.27

Figure 2. Hall characteristics, ohmic characteristics and transconductance of four samples.

The HEMTs that were tested had gate length and width of 1μm and 50μm, respectively. The gate–source and gate–drain distances were 1μm and 2μm.

The devices with AlN spacer and high-Al-content barriers had lower threshold voltages (i.e. more negative). The measured and intrinsic (i.e. minus contact resistance effects) transconductances were similar (Table 1). This is taken as an indication by the researchers that the saturation velocity of the 2DEG is not improved by the AlN spacer.

However, the transconductance is high over a wider region with an AlN spacer, and there is a tail into the region with gate voltages above +3V (Figure 3). Also, the maximum drain current at a gate voltage of +4V was 25–30% greater than without an AlN spacer. The researchers comment: "The obtained maximum drain current density was 1.3A/mm, which is sufficiently competitive with other reported values for AlGaN/AlN/GaN HEMTs. It should be noted that we could not have obtained these favorable results had the Si ion implantation doping not been employed in the fabrication of the HEMTs."

Breakdown performance was not affected by the AlN spacer — all devices tested at a gate voltage of −5V had increasing drain current (more than the gate current) beyond 50V drain bias, and breakdown occurred at about 150V. "We consider that these breakdowns occurred as a result of the relatively large amount of residual impurities in the deep-channel-layer region or buffer layer in all of present four epitaxial wafers, which are not associated with the AlN spacer layer and Si ion implanted region." All the devices also demonstrated similar current collapse effects in both DC and pulsed operation. ■

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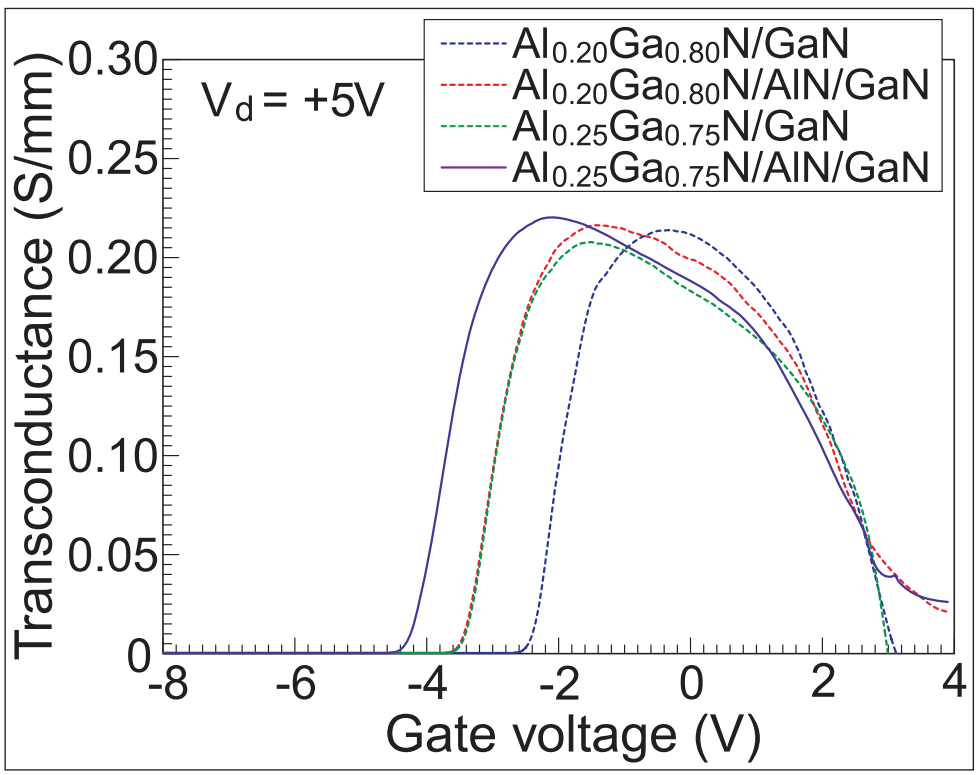

Figure 3. Gate voltage dependences of transconductance at drain voltage of +5V for the four HEMTs fabricated with Si ion implantation doping.