

GaN-on-Si opportunity for extending the life of CMOS silicon fabs?

Announcements of gallium nitride light-emitting diode samples produced on silicon in 150mm and 200mm facilities gives hope for others. [Mike Cooke](#) reports on the cost-reducing potential and obstacles faced by the industry.

Much of the recent effort to expand the scope of gallium nitride (GaN) and related semiconductor materials to more applications and markets has centered on developing epitaxial growth methods on silicon (Si) substrates. The drive behind this work is economic. Crystalline silicon is much lower cost (~\$0.1/cm²) than the alternatives such as sapphire (~\$0.8/cm²), silicon carbide (~\$6.6/cm²), and especially bulk or freestanding GaN.

Silicon could also enable another factor — ‘economies of scale’, where production in volume is much less expensive than making a few pieces. In particular, silicon wafers are available in diameters up to 8-inches. Actually, advanced CMOS production uses 12-inch diameter substrates (and some want to move to 18inch/450mm), but the crystal orientation is different — (001), rather than the (111) orientation that is most suitable for gallium nitride growth.

LED production on sapphire is carried out on wafers of at most 150mm diameter, with the majority being on substrates of 100mm or less. Silicon carbide (SiC) is similarly restricted to around 100mm diameter.

Another factor is that, as CMOS production migrates to larger substrates, older facilities become more desperate to fill production schedules at a profitable rate. Converting to GaN production could extend the useful life of such fabs.

These are some of the selling points, but there are also serious obstacles to lower-cost production. The attractions of GaN and related semiconductor materials

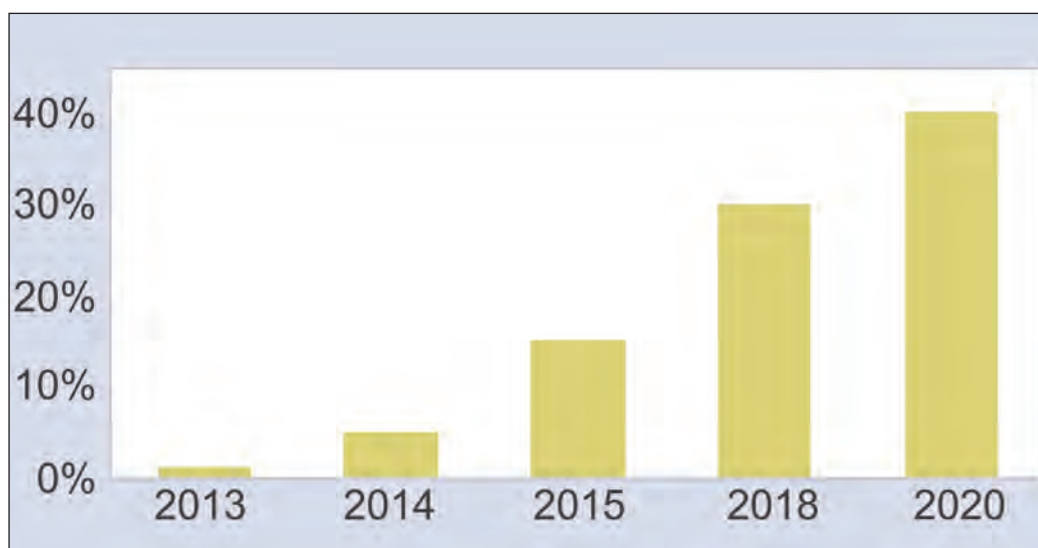


Figure 1. IHS GaN-on-Si LED market share outlook in terms of revenue for the packaged LED market.

— e.g. green, blue, violet etc light emission and high critical field for power transistors — are seriously impacted by defects that arise in the growth process. The density of defects tends to be higher when there is a greater mismatch with the underlying substrate. Unfortunately, the mismatch with silicon at 17% is higher than the alternatives: 16% for sapphire, 3.3% for 6H SiC, and 0% for GaN.

Also, the infrastructure of CMOS production is different from that of the light-emitting devices that presently form the bedrock of GaN-based mass production. While most of the processing steps of CMOS are in tools that process single wafers, the epitaxial growth equipment for LEDs and laser diodes handle large numbers of substrates at a time.

The single-wafer approach of CMOS was developed to enhance process control and thus increase yields of extremely complicated sub-micron devices. The structures of LEDs and laser diodes are much simpler,

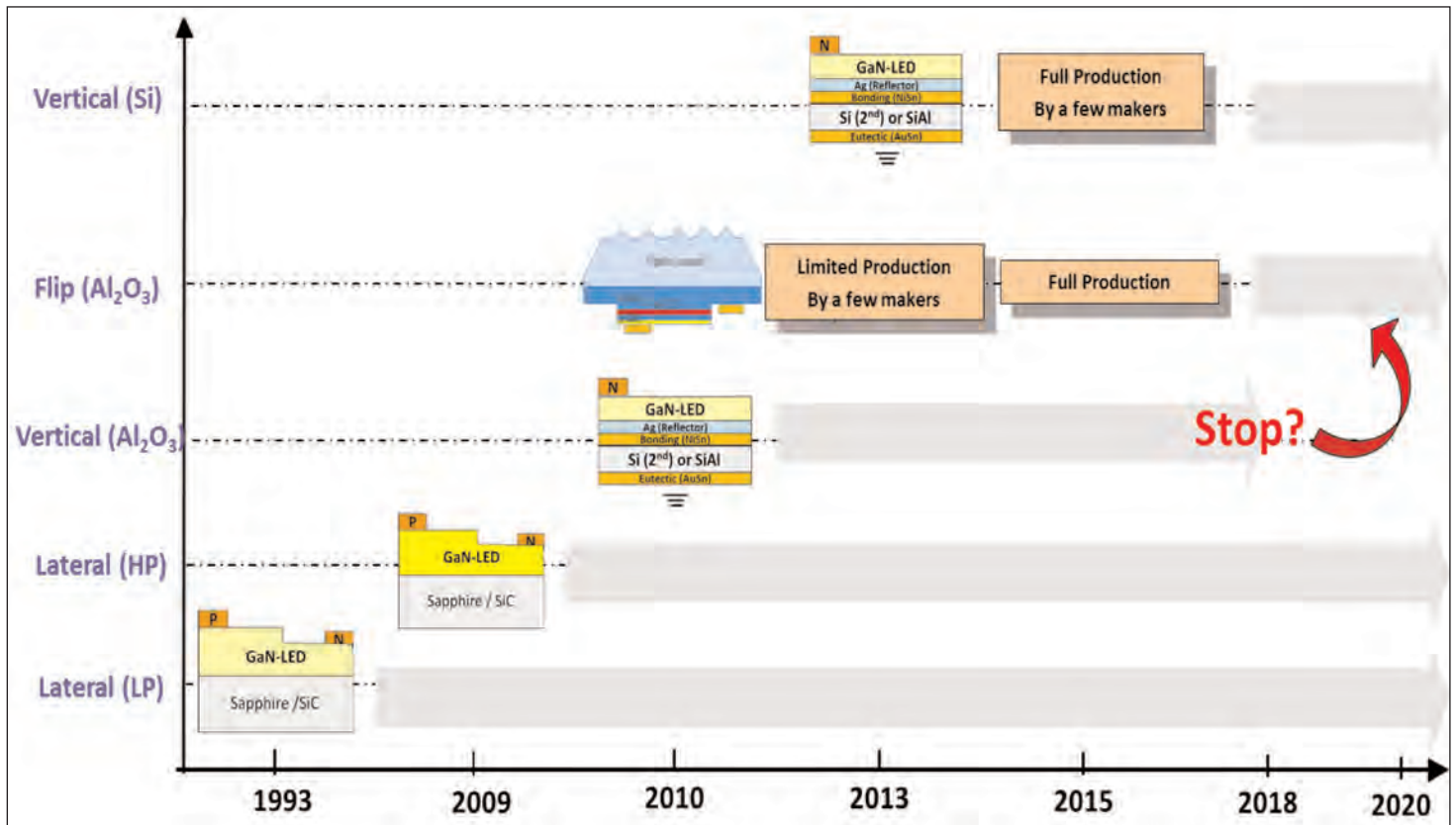


Figure 2. IHS projected roadmap for GaN LED production.

and there has not yet been a similar pressure for such exacting process control. As a result, batch-type processing is a more natural method to increase production volumes.

Despite the difficulties and obstacles to growth on silicon, research and development has progressed to the stage that samples from Japanese companies Fujitsu and Panasonic are beginning to appear in the power switching arena [for example, see Mike Cooke, *Semiconductor Today*, p82, November 2013]. These devices are normally off transistors produced on silicon with hopes of application in cost-sensitive power switching devices.

The more challenging light-emitting application has also begun to see commercial development, with Plessey and Toshiba both announcing samples of 'second generation' devices in recent months.

Market researchers at IHS Inc forecast that the share of GaN-on-Si wafers in the LED market (Figure 1) will increase at a compound annual growth rate (CAGR) of 69% between 2013 and 2020, reaching 40% of all GaN LEDs manufactured ['GaN LEDs on Silicon', November 2013]. Such high CAGRs are typical for 'hockey stick' graphs starting from a baseline near zero.

During 2013, the researchers estimate that 95% of GaN LEDs were produced on sapphire, while only 1% (~0%) were made on silicon. Growth in GaN-on-Si LED manufacturing is also expected to grab market share from silicon carbide substrates, which are often used for high-brightness devices because of the

material's superior thermal conductivity. Although silicon's thermal conductivity is somewhat less than that of silicon carbide, it is much better than sapphire's.

The market researchers believe that repurposing existing silicon manufacturing facilities for GaN-on-Si LED production would require minimal investment. "Many of the CMOS semiconductor manufacturers already have excellent inspection tools, unlike traditional LED companies," comments Dkins Cho, senior analyst for lighting and LEDs at IHS. "This could help increase their process yield through in-situ monitoring. However, it is unlikely the repurposing will happen overnight; instead we forecast a shift during the coming years."

However, there remain some challenges, according to IHS. Silicon strongly absorbs the radiation emitted from GaN-based LEDs and therefore creates difficulty for traditional lateral current flow chips that emit through the substrate (Figure 2). One way around this is to remove the silicon substrate. In principle, this has the added benefit of vertical current flow through the LED, which should improve efficiency. Unfortunately, the conventional laser lift-off silicon substrate removal process tends to reduce process yield.

Another analyst group, Lux Research, is less sanguine on the prospects for GaN-on-Si LEDs. In its June 2013 report 'Dimming the Hype: GaN-on-Si Fails to Outshine Sapphire by 2020', these researchers point out that sapphire is moving to lower substrate costs, improved wafer yields, availability of larger substrates and



Figure 3. Kaga Toshiba Electronics Corp, where Toshiba's GaN-on-Si LEDs are produced.

increased die throughput. "As a result, GaN-on-Si, with unproven performance and reliability, must race to stay relevant as the window of opportunity closes."

Both Plessey and Toshiba reflect IHS' assertion that GaN LED on silicon production will occur in repurposed silicon fabs.

Plessey in the UK acquired CamGaN, a spin-out from Cambridge University research, in December 2011. CamGaN's technical knowhow, intellectual property and patents have now been converted into commercial production at Plessey's existing 6-inch facility in Plymouth, UK. The company claims its 'MAGIC' trademarked devices deliver "industry-standard performance at a dramatically reduced cost of manufacture, with estimated savings of up to 80%".

The latest devices double the efficacy of its previous samples announced in February 2013. "We have a roadmap that puts MAGIC ahead of the efficacies achieved by sapphire-based LEDs and, thereby, sets a new milestone in terms of Lm/\$ performance," says Plessey's chief technology officer Dr Keith Strickland.

A variety of 'white' LEDs are sampling under the descriptions 'warm', 'neutral' and 'cool', with color temperatures in the range 2700–5500K. The color rendering indices are in the range 70–80 with 60mA injection current. The respective forward voltage is typically 3.2V. The luminous flux is in the range 7.9–12.3lm.

Meanwhile Toshiba boasts that it has developed a process that can produce GaN-based LEDs on 200mm-

diameter silicon wafers. The Japanese company also points out that it can use existing silicon facilities (Figure 3).

The new Toshiba device is a 1W 'white' product under the LETERAS trademark. The color temperatures range between 2700K and 6500K with color rendering minima of 80 and 70, respectively. The luminous flux range is 104–135lm. These devices run with a 350mA injection current and forward voltage of 2.85V.

Researchers from Toshiba reported at the 2013 International Electron Devices Meeting (IEDM) in December on a method for reducing threading dislocation densities in 200mm GaN-on-Si wafers by using silicon nitride multiple-modulation interlayers. Early in 2013 Toshiba acquired the GaN-on-Si technology and related assets of California-based LED chip and lighting array maker Bridgelux Inc.

Another company that has been developing GaN on Si is Azzurro Semiconductors in Germany. In particular, it has been focusing its recent research effort towards providing 150mm epitaxial template wafers for GaN-based LED production. The company says that its wafers are suitable for standard Si-semiconductor equipment in terms of wafer size, low bowing and opaqueness. Company researchers have been reporting promising results in the past year [see Mike Cooke, *Semiconductor Today*, p78, October 2013].

The metal-organic chemical vapor deposition (MOCVD) tool manufacturers are also working on

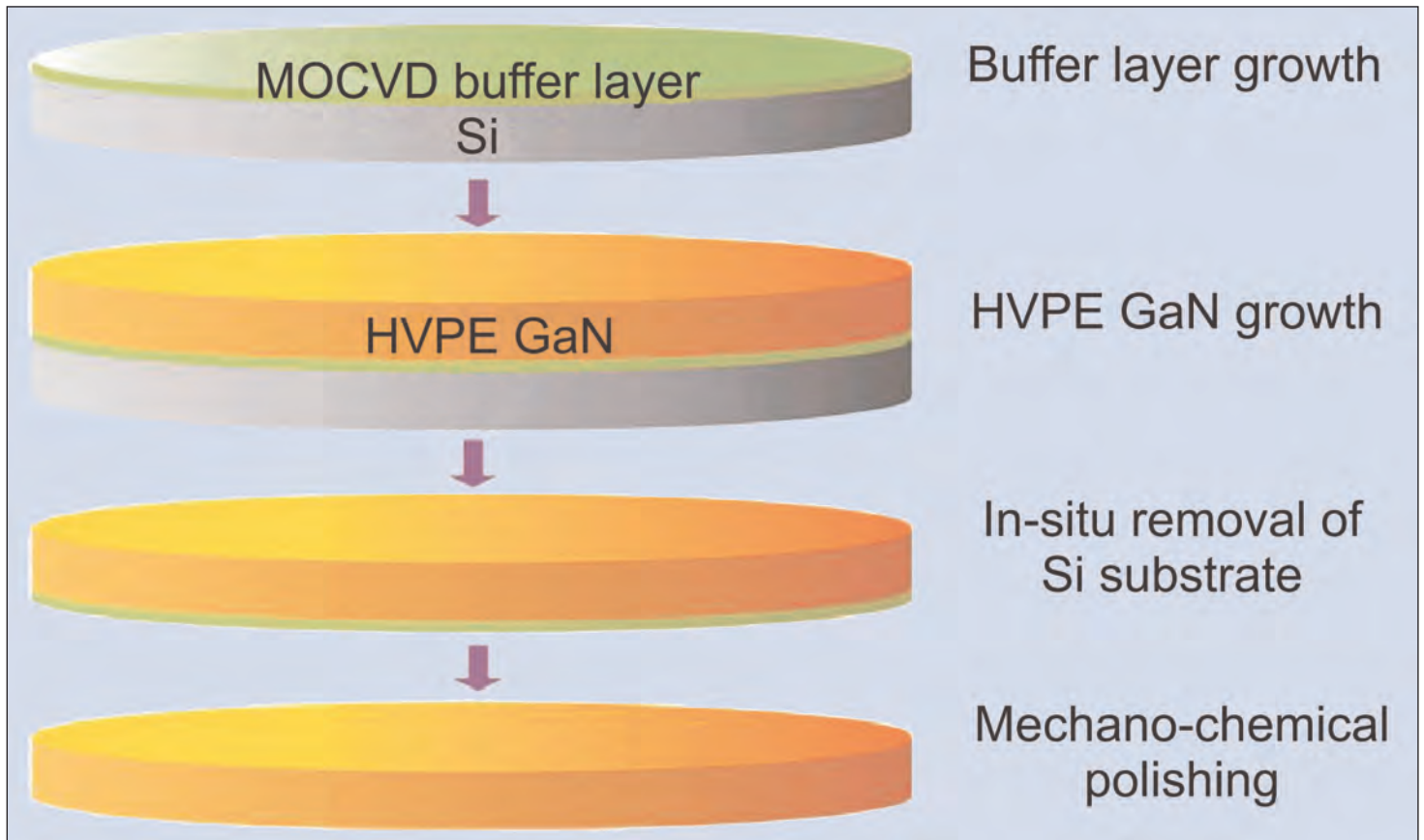


Figure 4. Schematic Samsung/SNU process steps for fabricating freestanding GaN-on-Si substrate using in-situ Si etching.

meeting the needs of this potential new market.

Although Veeco's sales effort for GaN-on-Si equipment is presently focused on power electronics applications, the company announced in September 2013 a collaboration agreement with the Belgium-based research center Imec. However, the two organizations have been working together on GaN-on-Si since 2011. The aim is to lower the cost of production of GaN-on-Si power devices and LEDs.

Jim Jenson, senior VP, general manager, Veeco MOCVD, comments: "This technology can be used to create lower-cost LEDs that enable solid-state lighting, more efficient power devices for applications such as power supplies and adapters, PV inverters for solar panels, and power conversion for electric vehicles."

Aixtron supplies the University of Cambridge with MOCVD equipment for research that includes GaN LEDs on silicon. The commissioning of an Aixtron Close Coupled Showerhead (CCS) MOCVD reactor capable of handling 150mm wafers at Cambridge was announced in April 2013. Plessey is another customer of Aixtron. The company also supplies GaN-on-Si MOCVD equipment to a number of companies focused on power switching/conversion electronics.

Aixtron has also set up a training and demonstration center at the Suzhou Institute for Nanotechnology and Nanobionics (SINANO), which works on LED and GaN-on-Si research.

An interesting new development is the prospect of the production of high-quality freestanding GaN on silicon. Researchers at Samsung Electronics and Seoul National University (SNU) in Korea produced high-quality freestanding GaN substrates from hydride vapor phase epitaxy (HVPE) on silicon templates [Moonsang Lee et al, Appl. Phys. Express, vol6, p125502, 2013].

HVPE is a faster growth process for GaN than MOCVD, allowing layers of $\sim 100\mu\text{m}$ rather than $1\text{--}10\mu\text{m}$ to be produced. Usually, the substrate with the seed GaN layer needs to be more nearly lattice matched than silicon to obtain high-quality material. Also, problems such as cracking can occur when the foreign substrate is removed to give freestanding GaN.

The main difference with normal attempts to grow freestanding GaN on silicon is that, instead of waiting for the material to cool, the Samsung/SNU researchers separated the GaN from the silicon substrate at high temperature.

Growing high-quality GaN on silicon should lead to larger-diameter wafers and therefore economies of scale. Although the experimental work was carried out on 2-inch silicon wafers, the researchers believe that production on 8-inch diameter substrates should be possible in the near future.

High-temperature separation of the substrate avoids a problem arising from the different rates of thermal

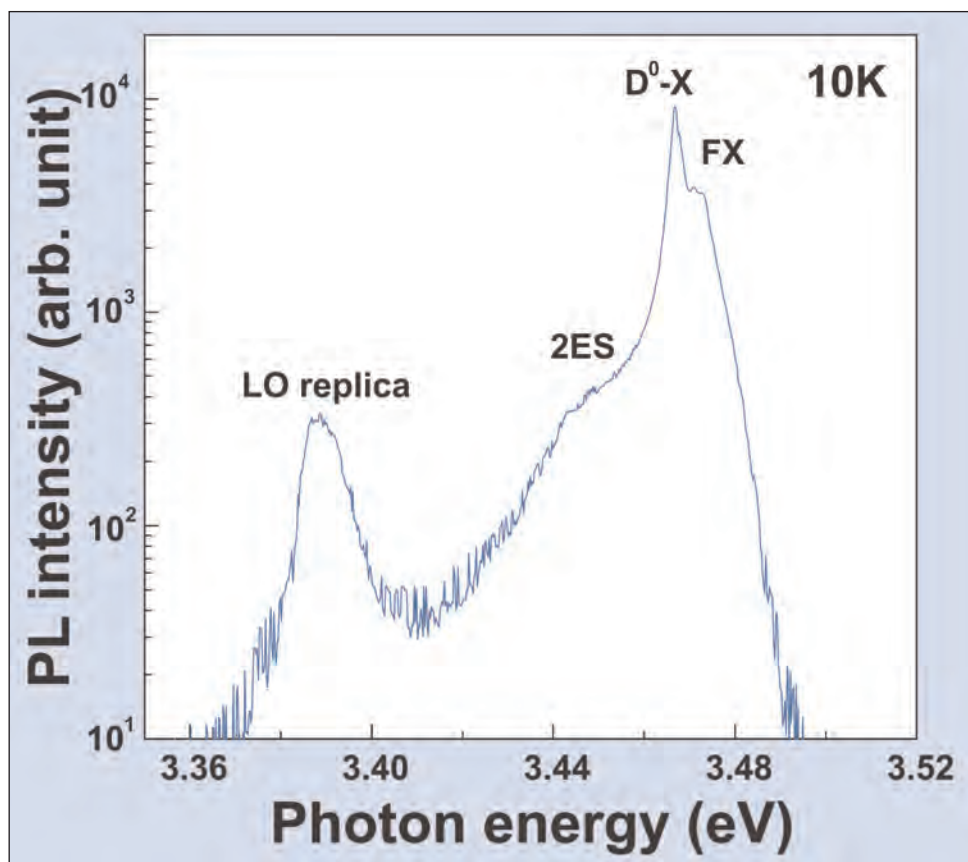


Figure 5. PL spectrum of Samsung/SNU freestanding GaN at 10K: FX is attributed to free exciton; D^0-X is neutral donor bound-exciton; 2ES is second excited state; LO replica is longitudinal optical phonon replica.

expansion of $5.59 \times 10^{-6}/K$ for GaN and $3.37 \times 10^{-6}/K$ for silicon. As the grown GaN material cools to room temperature on silicon, the different rates of contraction lead to cracks and bowing of the wafer.

Simulations suggested that, while the mismatch with silicon causes tensile stress in GaN at room temperature, above $900^\circ C$ the GaN layer experiences mild compression. The researchers therefore believed that removing the silicon at high temperature could avoid the cracking and defect problems often found in producing freestanding GaN.

In the Samsung/SNU method (Figure 4), the 2-inch (111) silicon wafer was first cleaned to remove oxygen and to give a hydrogen-terminated surface. Buffer and transition layers were grown using MOCVD.

The buffer consisted of 100nm aluminium nitride (AlN). This layer reduced lattice mismatch and prevented silicon from diffusing from the substrate into the nitride semiconductor layers — an effect known as ‘melt-back’ that inhibits GaN growth.

The transition layer was a series of aluminium gallium nitride (AlGaIn) layers with a “unique epitaxial structure” developed by Samsung along with researchers from Sejong and Hanyang universities [<http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=1385248>]. The structure is designed to reduce dislocations and compensate for stress during growth.

The MOCVD processing was completed with a 500nm gallium nitride (GaN) layer (250arcsec x-ray rocking curve).

The HVPE of 400 μm of GaN was carried out in a chamber that was also capable of in-situ etching. The HVPE process consisted of pre-reacting hydrogen chloride (HCl) with Ga liquid to form GaCl gas. The gas was transported to the growth zone at $1000^\circ C$ to react with ammonia (NH_3) to give GaN deposition on the MOCVD template. Nitrogen was used as a carrier gas for the HVPE.

The process was completed by etching away the silicon substrate at $1000^\circ C$ using HCl gas. The reactor was then cooled to room temperature to yield the freestanding GaN. Microscopic inspection of the product showed an absence of cracks or defects such as melt-back and pits.

The (0002) x-ray rocking curve gave a peak with full-width at half maximum (FWHM) of 65arcsec for the Ga face and 200arcsec for the N-face. The difference is attributed to bowing and the fact that the N face

comes from material at the junction with the MOCVD template layers. However, the amount of bowing is much reduced at about $20\mu m$, compared with the hundreds of microns typical for freestanding GaN produced on foreign substrates that are removed at room temperature.

The estimated pit density after 30 minutes etching in phosphoric acid (H_3PO_4) was less than $10^6/cm^2$ over the whole wafer. This value is comparable to or better than for thicker material ($\sim 1mm$) grown on sapphire. Low etch pit densities indicate a reduced numbers of dislocations.

Photoluminescence (PL) at 10K (Figure 5) showed an edge peak close to that of freestanding GaN produced on sapphire. The researchers see their photoluminescence results as confirming the high crystal quality. However, the neutral donor bound-exciton (DBE) transition (D^0-X) at 3.467eV (FWHM 3.1meV) is slightly red-shifted compared with strain-free ammonothermal GaN or material from homoepitaxy. The researchers see the red-shift as indicating slight tensile stress in their freestanding GaN from residual strain due to the quality difference of the Ga- and N-face surfaces. ■

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